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## Acoustic LP filtering for High Frequency Spurious Harmonics Rejections

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## ACOUSTIC LP FILTERING FOR HIGH FREQUENCY SPURIOUS HARMONICS REJECTIONS

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### I. INTRODUCTION

With the implementation of 5G and other Radio technologies, a modern handheld device can include and operate multiple Front-End module (FEM) devices. Those can support applications such as: LTE, NR, WCDMA, BDS, GPS, GNSS 2.4GHz Zigbee, Thread, Bluetooth, WiFi 6/6E – 802.11ax (operating at 2.4 GHz ISM band), Wi-Sun, UHB, UWB amongst others. In many cases, the system architecture makes use of more than one module on each phone board for diversity Receive. The above applications range in frequency from 400MHz to 8000MHz, operating with different power requirements making use of FDD, TDD, and CDM schemes.

One of the biggest design challenges faced by the combination and coexistence of all these systems on a single phone board, is the interference from the generated harmonics and Intermodulation products. Many of the components used in the system exhibit a strong non-linear behavior, resulting in high power generated harmonic signals. Such components are the PA, BAW and SAW filters as well as the Switches [1-5]. For example, the H2 products of a B66 or B3, B25, B1 fall in n77 and n78 range. The H2 products of n41, fall in the Wi-Fi spectrum. The higher (H3, H4 etc.) products of many other bands, including the Wi-Fi, are falling in the UWB spectrum. That interference often creates RX sensitivity issues that limit the End Users Device performance and experience.

Solutions currently employed to address this issue focus on suppressing as much as possible the PA and acoustic filter self-generation by implementing additional filtering at the Multiplexing Network with LC tanks, implementing LC notch filters at the Switch outputs or the PA output in conjunction to matching components etc. In Fig. 1 the block diagram of a Full Mid-High Band Multiplexing Network is shown, where a Multiplexing Switch is used to implement the CA combinations needed at the output and a post ASM Harmonic trap is designed at the output of the ASM.



The post ASM Harmonic trap can be implemented with a combination of laminated implemented elements and SMDs, components integrated in the ASM die or an integrated passive circuit. In many module architectures, multiple antenna outputs are needed, therefore such a trap is needed for each of the outputs. For the architecture seen in Fig. 1 two circuits as such are used.

In most of the cases such solutions have been effective as have been targeting a very specific frequency range, and an additional rejection in the order of 10-12 dB could suffice. In more recent applications, such solutions are not as effective, as the rejection requirements become higher and the frequency range very wide. That in combination to the fact that any additional component added in the chain increases the overall path losses, resulting in higher NF and current consumption, these solutions are becoming less desirable not to mention the BOM cost increase due to the additional SMD components.

Figure 2 illustrates another post ASM trap circuit implemented on a MHB platform comprising a shunt inductor, a series inductor with a capacitor in parallel and a shunt capacitor in series to an inductor. On the module two identical implementations are used, one for each Antenna output. For this MHB platform, a combination of SMD capacitors and inductors and laminate integrated inductors was implemented.

## II. DISCUSSION

A different approach is proposed here where a BAW based Low Pass filter is implemented at the output of an RF module to suppress all the spurious harmonic products, with minimum impact in chain loss. An LC filter, which uses BAW resonators with Q of  $\sim 1000$ , can present rejection levels more than 30dB in a wide frequency range, while minimizing the path losses.

Such a filter implementation can use one or more BAW resonators in combination with Inductors. The Inductors can be implemented in the laminate section of can be SMD devices, even IPD. The topology of such LP filter apparatus, comprising 3 BAW resonators in combination to 2 Inductors in series is seen in Fig. 3. The BAW stack and resonator types were chosen to achieve a certain rejection level for B66T H2 starting at 3.5GHz. The series inductors are also simulated as lumped elements with a Q of 30.



Fig. 3 illustrates a Low Pass filter using three BAW resonators in Shunt and two series inductors. This BAW based LP filter is designed for a platform where H2 rejection requirements are stringent and a post ASM filtering is implemented to improve the H2 and H3 rejection. That is compared against the final implementation on the platform which is based on the circuit described in Fig. 2.

The Insertion Loss response of the LC type filter including the ASM is plotted in Fig. 4 with the black trace. On the same plot, in red trace, the response of the BAW based LB filter described in Fig. 3 is plotted. As shown in the plots, the BAW based filter has a steeper rejection at 3500MHz presenting less IL at frequencies below 3GHz. The overall rejection for the B66T Second Harmonics is below 15dB for the full frequency range, where the alternative has a narrower notch at those frequencies. In addition to the red trace presents rejection better than 30dB from ~5 GHz to 9, suppressing all higher mode harmonics where the LC implementation shows a significantly worse rejection for higher frequencies.

Such a BAW based LP filter can be implemented for each of the Antenna paths of the module using the same filter die. That can minimize the space needed as well associated costs.

Alternative embodiments of the BAW based LP filter are shown in Fig 5. Those can utilize 1 or more BAW resonators in shunt as well as 1 or more inductors in series. In the implementation shown in Fig.5 A, an inductor is used in parallel to one of the shunt BAW resonators. In the embodiment illustrated by Fig. 5B, an inductor in series is connected to a BAW resonator. On a different topology, seen in Fig 5.C a BAW resonator is connected in parallel to one of the series inductors. Variations of these topologies can be derived and adjusted to the needs of the corresponding application.

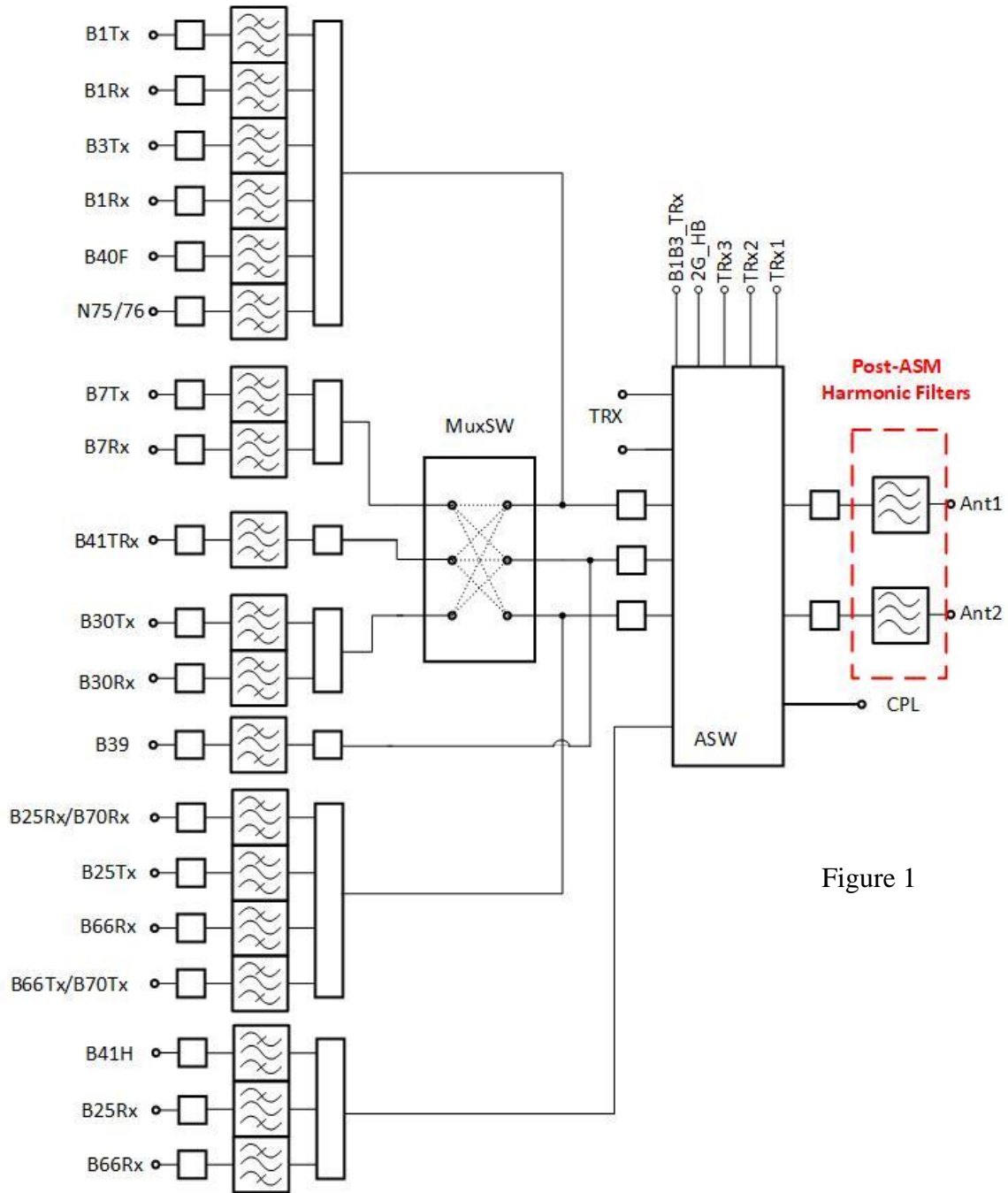


Figure 1

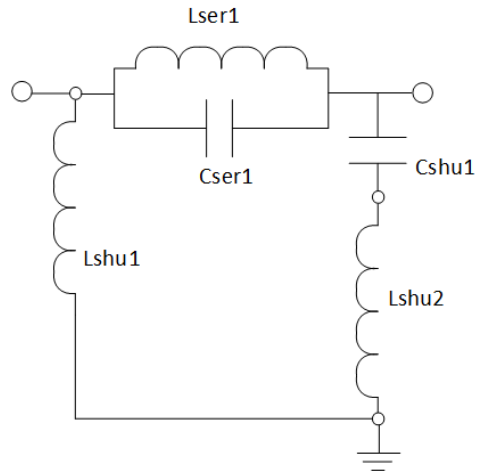


Figure 2

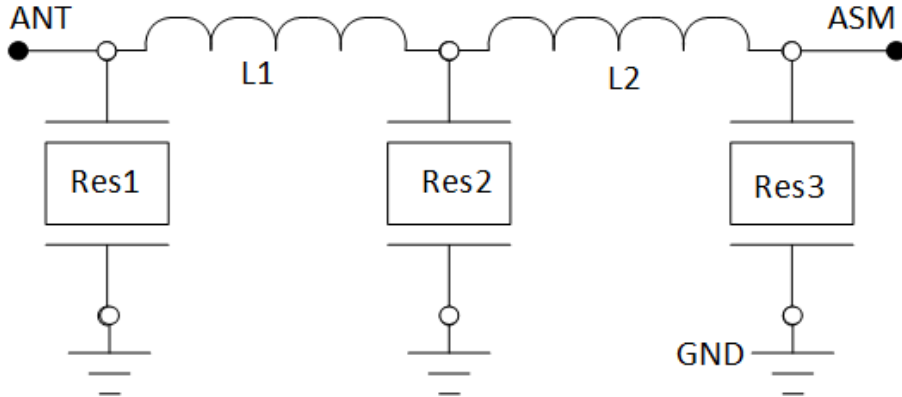


Figure 3

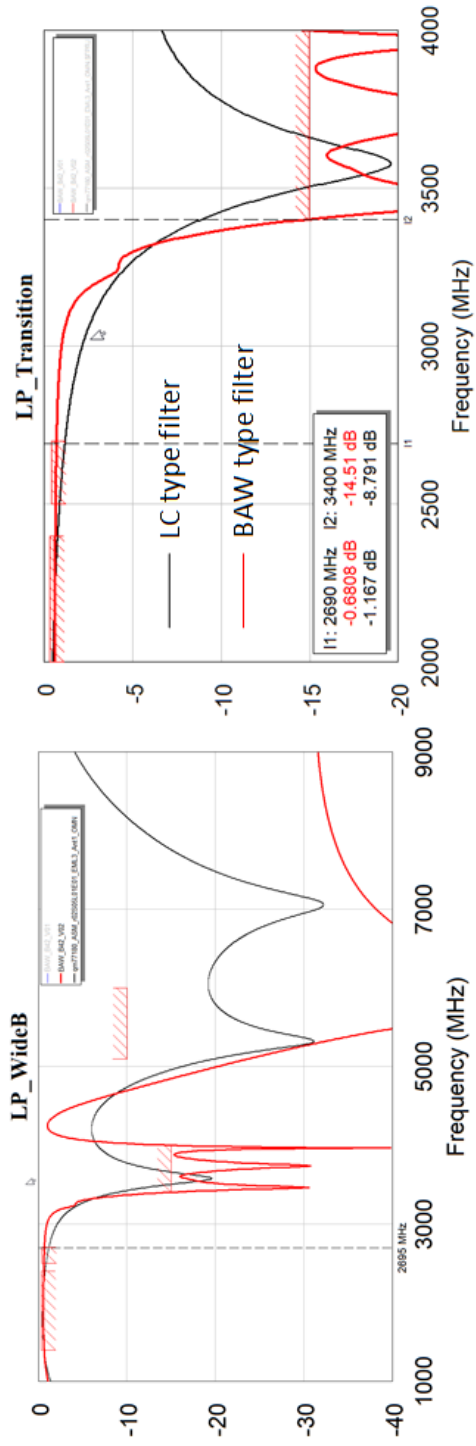


Figure 4

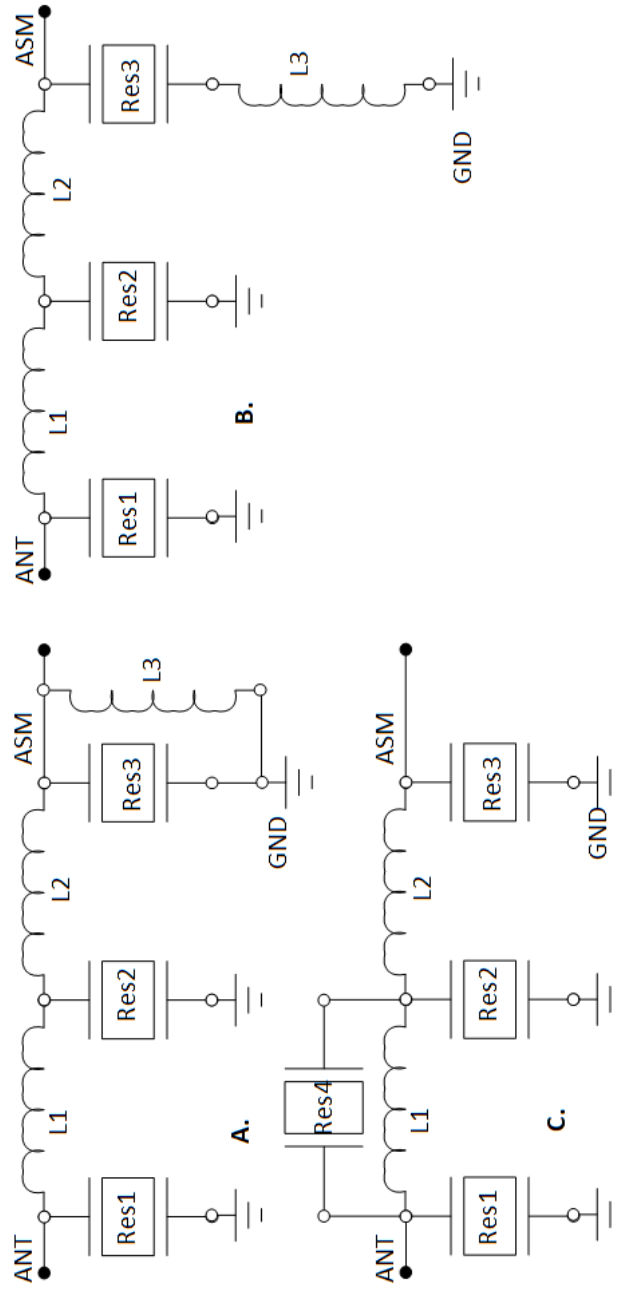


Figure 5