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Enhanced LNA Control Methods and Circuit Techniques

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I. INTRODUCTION

Pressure to reduce LNA power has led to design tradeoffs resulting in increased manufacturing variability. Determining and maintaining optimized tuned operation across operating modes is increasingly complex and time consuming for production test. The primary goals of this development are to both mitigate these challenges with enhanced performance & robustness as well as reduce area & power. This disclosure details how this was achieved and demonstrates the simple compatibility with existing designs & processes.

Common gate LNA design typically follows a scheme of generating reference current, distributing programmable current for I to V conversion and finally maintaining the tuned current density and bias voltage for a given LNA band of interest. Note that the RC network on LNA gates have no impact on DC bias but will become important in later sections of this disclosure.

Calibration is performed manually. Either LNA drain current or the sum of LNA drain + LNA bias current may be adjusted via PTAT resistance control cs_trim. Ideally cs_trim would shift only due to resistor skew. In practice cs_trim dominantly is shifted due to more dominant reference + LNA mismatch. It is apparent that trim range provided by N bit cs_trim must be sufficient to compensate for total skew and mismatch errors which lead to significant variation in core LNA performance. A non-ideal tradeoff of this approach is that the consequence of shifting master current reference (Iptat) to recenter LNA drain current (Idrn) leads to deviation of bias voltage.

Ideally the LNA reference would fully replicate the current and voltage headroom conditions of the LNA core. Referring to the figure above, the LNA core composed of transistors T0 and T0c is optimized in geometry and current density for RF performance. The ratio of reference current to core current M is maximized in order to save power. Maximizing this ratio means extra care must be taken to properly manage systematic offsets and manufacturing variations between reference and core. Further reducing power by making CG current significantly lower than CS current leads to device operating differences between CG reference, CS reference and core. Collectively these differences lead to challenges in finding calibration targets that are held for all operating modes.

A brief analysis of the reference circuit behavior is helpful to understand the unwanted interactions of the CS and CG bias. Figure 2a is a simplified example of a reference bias scheme involving an independent pair of stacked diodes connected transistors. Node A voltage is the gate to source voltage (Vgs) of T1 as a function of current from the CS DAC (Ics). Due to finite output impedance (rds) the current of T0 will be a function of its drain voltage at node B. LNA cascode T0c sets the voltage at node B. It is at this point that we encounter the first sensitivity in this scheme. The voltage at node B becomes a function of both CG DAC current (Icg) and T0 current.

In saturation Vds > (Vgs – Vth) and (Vgs – Vth) is overdrive voltage or Von. Ignoring finite device impedance the fundamental relation between current and voltage is:

$$Idsat = \frac{1}{2} K \frac{W}{L} (Vgs - Vth)^2 \quad and \quad Vgs = \sqrt{\frac{2IdsatL}{KW}} + Vth \quad and \quad Vgs = Von + Vth$$

Although small signal impedance into the drain of a diode connected device is approximated $1/_{gm}$ applying a current to a diode connected reference gives a corresponding change in Von that is proportional to the root of the change in current. If the tradeoff is made to use independent Ics and Icg currents the core and bias interactions become quite complex. The purpose of the CG control is to hold node voltage B to a known value however node B is a function of more than two factors- since Vgs of the cascode devices is a function of drain current differing current densities and differing device layouts lead to systematic offsets which are further impacted by mode of operation. As demonstrated in Figure 2b there is a feed forward operation in which the CG DAC is attempting to provide a voltage at T0c’s gate in order to set node B, however without matching Ics/Icg it is not unlike simply using an I*R bias CG scheme.

In the prior analysis channel length modulation was neglected. In practice nanometer thin oxide devices are used in the LNA for both CS and CG devices and these have non negligible intrinsic impedance rds. Moreover, the scaling ratio M is typically implemented with non-unitized core devices. For instance, a reference CS device may be 12um and implemented with a 3-finger device. In order to minimize parasitics a 240um CS core device may be implemented with a 60-finger device. So rather than 20 replicated instances of the 12um reference device the tradeoff is made to accept the systematic offset and increase sensitivity to mismatch.

In Figure 3, an ideal feedback loop is used to demonstrate the significant impact of aggressive scaling to reduce power in the reference. Devices are nominal with 0 mismatch. An ideal constant to absolute temperature (CTAT) Ics current is provided. The ideal amplifier uses feedback to keep Vdrn constant and independent of Ics while adjusting Vgs. At the same time an ideal voltage source is connected to the CS device on right. The drain current of the CS device is plotted for two scenarios simulated in s8w SOI. Given M=20x as drawn if 400uA is provided by the CS DAC 8mA is expected at the CS device drain. If 20 copies or iterated instances of the reference are used the resulting CS current is on average close to the expected 8mA although has a slight negative to absolute temperature (NTAT) slope. In the second scenario a single device with 60 fingers is simulated producing nominally 10.25mA which is a 28% error. In addition, the sensitivity to temperature grows along with the systematic offset error. There are a number of physical factors that contribute to the errors when scaling with fingers rather than iterations, but accuracy boils down to the degree reference replicates core. Both I and V bias as well as layout.

Figure 4 uses an 8sw two stacked diode bias scheme. Again nominal devices are used with 0 mismatch. Ics comes from a PTAT & CSDAC bias but is constant while the CG DAC sweeps Icg. Since this is feedforward the voltage at node A is conveyed to node B and voltage at B is plotted far right. The error from voltage A to B is shown on bottom left. As Icg/Ics → 1 the error decreases asymptotically approaching ~40mV. For simplicity degeneration resistance is removed but presence of degeneration resistance adds yet another layer of uncertainty between reference and core matching.

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II. DISCUSSION

An improved bias architecture for SOI and CMOS LNAs compatible with existing LNA products. The innovations provide all the following advantages with no known negative tradeoffs:

1. Provides independent control of LNA current and voltage
2. Reduces power & area while not impacting noise & performance
3. Simplifies calibration and improves yield
4. Ideally suited for advanced nanometer processes and beyond

Typically, an LNA is controlled with a pair of current DACs. The current source or CS DAC to set LNA drain current and a common gate or CG DAC to set terminal voltages for desired headroom. The scheme shown in Figure 5a is innovative because it allows current and voltage to be independently controlled in a linear step. Further benefits of the new approach are due to more accurately replicating core operating current density and voltage in the reference.

There are three techniques employed to make the overall scheme attractive. One is using a folded cascode bias for low voltage supply operation that also matches CG drain voltage between reference and LNA core. Two is creating a linear voltage reference to control CG device T0c gate voltage. Three is simple opamp servo to hold CS device T0 drain voltage constant independent of CS current.

Figure 5b is an example of employing the folded cascode technique in two locations. P type transistors Tp are provided with gate bias vgp so that nodes E, D, C and F are all equal and held at a value relative to supply vdd. There are a number of important benefits. One the bias voltage is a better replica of core voltage. Two current DACs headroom is constant and independent of DAC current or Vgs of N type diode connected devices. Three headroom of cascode devices T2c and T1c are independent of N type Vgs so remain in saturation. Figure 5c is a typical low power bias scheme also known as a flipped voltage follower. The top cascode device is used to set the drain voltage of bottom devices independent of bottom device Vgs and bias current. If Vgs1 is sufficiently large cascode device 2 will have sufficient Vds to remain in saturation. If not, then device 2 will operate in the linear region with Vds2 < (Vgs2 – Vth).

The previous example is a telescopic cascode circuit with two transistors in series. Now consider the example in Figure 6a. Left side is again telescopic but third device placed to set drain voltage of device 2. In case of small Vgs1 the gate1 must be level shifted for adequate headroom on the three devices adding complexity and not typically practical with today's supplies. The circuit on far right implements the same function and is more practical. The 3 stack telescopic third device is replaced with folded P device Tp requiring very low bias current. Device Tp contributes negligible noise while keeping headroom of device 1 & 2 independent of Vgs1 and current in device 1.

A negative tradeoff of defining the Vcg by applying current to diode connected FET is that the Vcg is proportional to root of the current. Therefore a greater current range is needed to support a given voltage range. Figure 6b places linear voltage reference Vcg to define T0 drain voltage. Vcg = Vb + Vgs. It is clear that if Vcg is properly adjusted across PVT and full current range that Vb will be constant.

Figure 6c demonstrates one way to implement a precisely defined voltage at node B by automatically adjusting gate of T1c. Now to the first order drain voltage of T0 and T1 is a replica of Vdrn. Local feedback to the opamp adjusts Vcg to compensate for PVT and terminal bias voltages independent of bias current. Having introduced a feedback loop the loop stability must be ensured. Here an important observation is made regarding Rcg and Cg of the LNA.

The common gate (CG) bias uses a sufficiently large value of Cg so that Cg acts as a voltage source holding the DC gate voltage of T0c. Rcg is typically on the order of KΩ to further isolate DC bias from RF when the LNA is in active gain mode. Placing the feedback operation on the CG bias rather than CS bias is most ideal because component arrangement of Rcg and Cg provide a zero making the loop inherently stable. To understand this consider that as frequency increases Cg becomes a short and looking out from the opamp into Rcg the opamp sees an impedance that plateaus at real resistance Rcg. In practice an additional capacitor may be placed on the gate of T1c in order to increase the gain margin of the loop. In doing so the loop gain continues to decrease as frequency increase however phase margin is > 90 degrees. There are two more benefits of placing feedback at the cascodes T0c, T1c rather than currents source devices T1, T0. First the cascode devices with or without opamp contributes little noise since CS devices dominate noise of the circuit.

Second placing feedback on CS device introduces many more additional variables. Consider Figure 7a. A typical value for Crf may be 10pF and the LNA RF input may be applied to the right hand plate of this capacitor. It cannot be assumed that Zsrc will be 50Ω for all frequency. Often a bandpass filter is used and typically the out of band impedance is not well controlled.

Since the Zsrc(f) can be unknown it is difficult to guarantee that the feedback loop will be stable for all input networks. This could lead to conditional stability. Therefore placing feedback on the LNA cascode device is the more robust option. There is much less sensitivity to rx input network and there is no need to add additional components to meeting the Nyquist stability criteria.

Yet another consideration settling time for power up and transitioning between LNA modes of operation. Again since rx input network is an unknown factor feedback involving CS device may present challenges in maintaining a critically damped transient settling response. Voltage feedback involving the cascode or CG devices is less sensitive to dynamic transient current.

Area and Power Reduction

Returning to classical approaches to LNA bias and referencing the analysis in the prior background section of this disclosure we note that to reduce manufacturing variation and yield loss two current gains must be minimized. First the ratio M of LNA drain current to CS bias current. Second the ratio of CS DAC current to CG DAC current.

Figure 7b illustrate an LNA and its bias resemble a basic current mirror. Output current variation relative to reference current is directly impacted by ratio M. As reference area and current is reduced to decrease power LNA drain current error will increase. For example if the ratio of reference current to output current is ¼ : 1 this will have 2X more error than if the ratio is 1:1.

A less obvious limitation to minimizing CG DAC current is that it becomes increasingly prohibitive to scale the CG bias. If CG bias is aggressively scaled down this leads to higher sensitivity to channel length modulation which means the LNA voltage headroom is difficult to control across gain modes and LNA drain current variation as a function of voltage increases. As a result of these tradeoffs often the required solution is to sacrifice power and area by using larger CS DAC currents. It follows that CG DAC current is also increased to more closely match CS DAC current.

One way to avoid this limitation is to replace the CG bias with voltage reference Vref. In this way the CS and CG bias are made independent. Moreover the CG DAC current may be scaled aggressively by leveraging lower power and low offset design. There are many options for generating Vref including using a bandgap or bandgap over poly current. Only few are discussed herein for sake of brevity.

A straightforward approach is to use long channel current source elements in the CG DAC along with larger area resistor elements as shown in Figure 8a. In any case the CG bias is simply converted to a linear voltage DAC. Another subtle but equally effective technique is to generate Vref by pushing a current into a resistor voltage divider connected between supply and ground as shown in Figure 8b. There are a couple of interesting traits to this technique. One is that when CG DAC current is 0 the minimum level of the voltage DAC is provided to opamp. As long as supply noise is filtered the upside is at startup or gain transition the feedback loop will be faster. Another is DAC current to voltage is I * resistors in parallel. Therefore current variation sensitivity is attenuated due to a lower effective load resistance.

In summary the disclosed embodiments simplify the tradeoffs in controlling yield. With proper design of the CG bias voltage reference and opamp the dominant source of systematic offsets and variation will be dominated by the ratio of LNA T0, T0c area to that of the reference device T1, T1c area. Just as with simple cascode current mirror a straightforward design tradeoff is exchanging more area and power for lower variability.

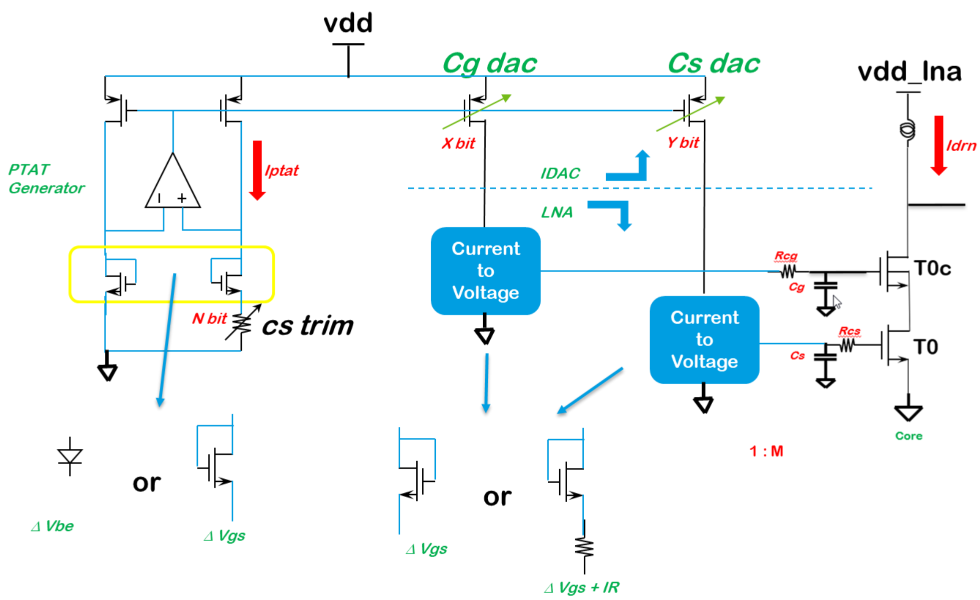

Figure 1

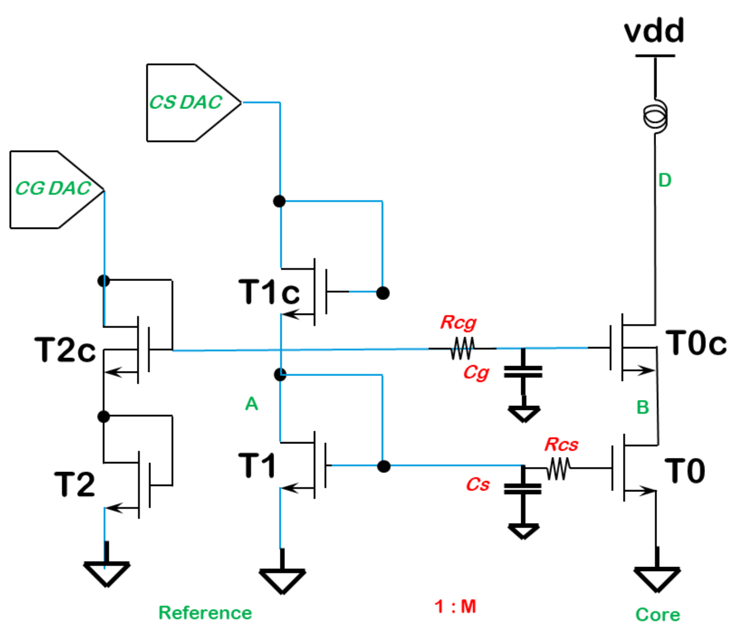

Figure 2a, 7b

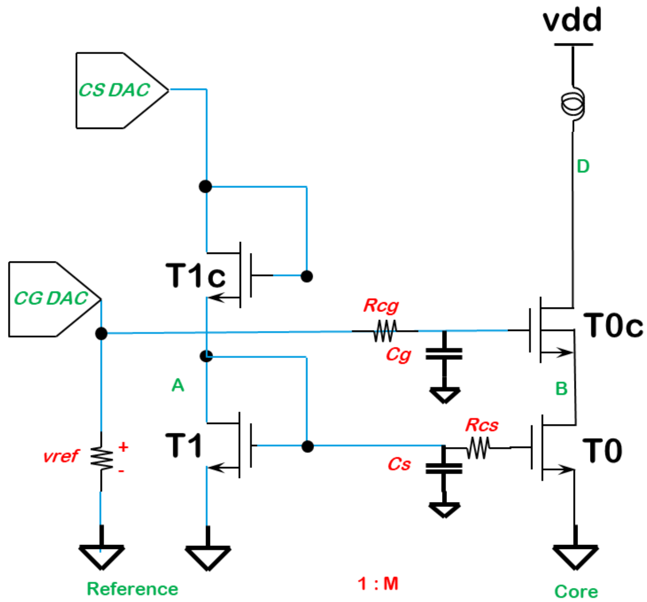
vdd
CS DAC
D
T1c
CG DAC
Rcg
T0c
Cg
A
B
T1
Rcs
T0
vref
+
-
Cs
Reference
1 : M
Core

Figure 2b

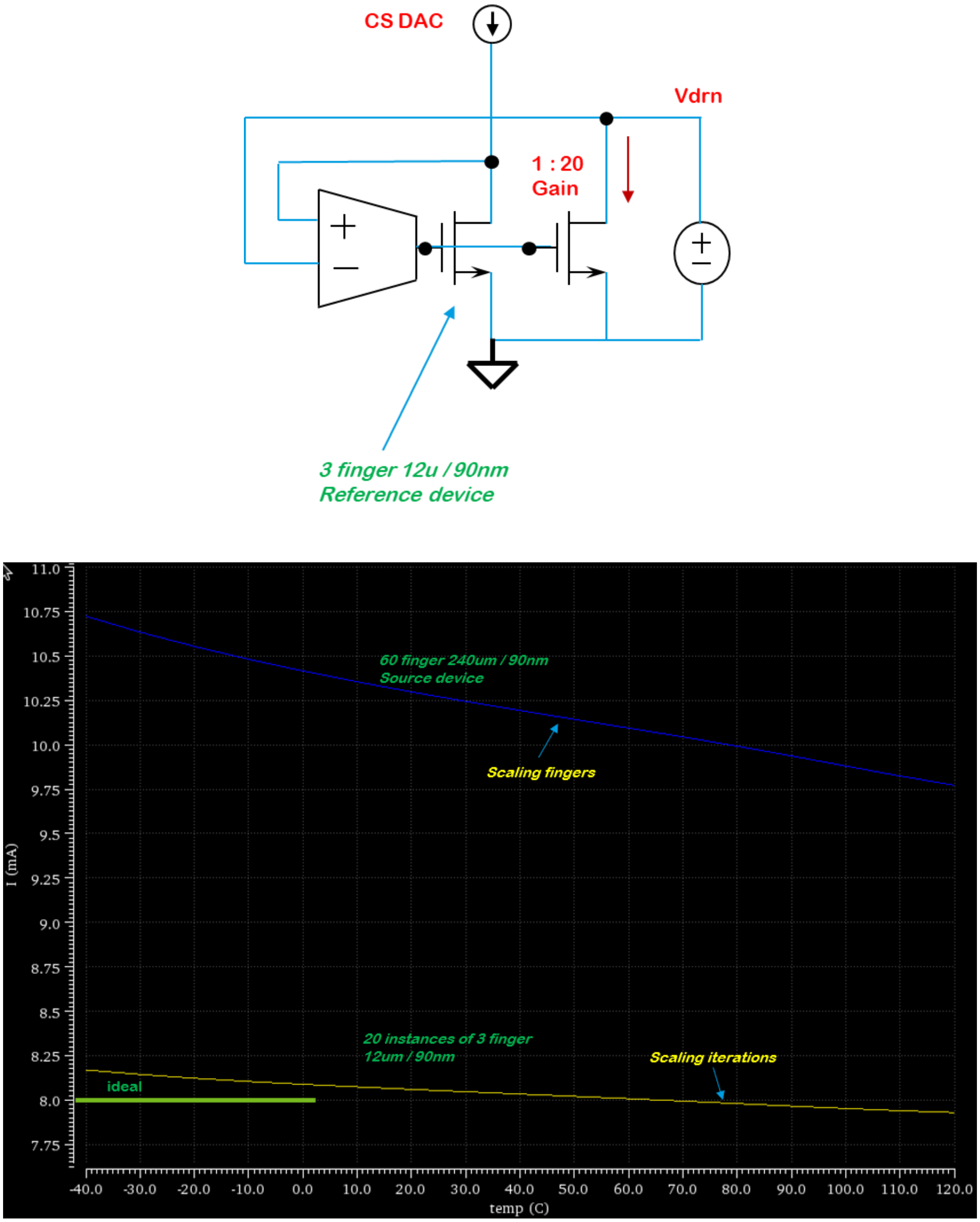
CS DAC
Vdrn
1 : 20
Gain
3 finger 12u / 90nm
Reference device
60 finger 240um / 90nm
Source device
Scaling fingers
20 instances of 3 finger
12um / 90nm
Scaling iterations
ideal
I (mA)
temp (C)

Figure 3

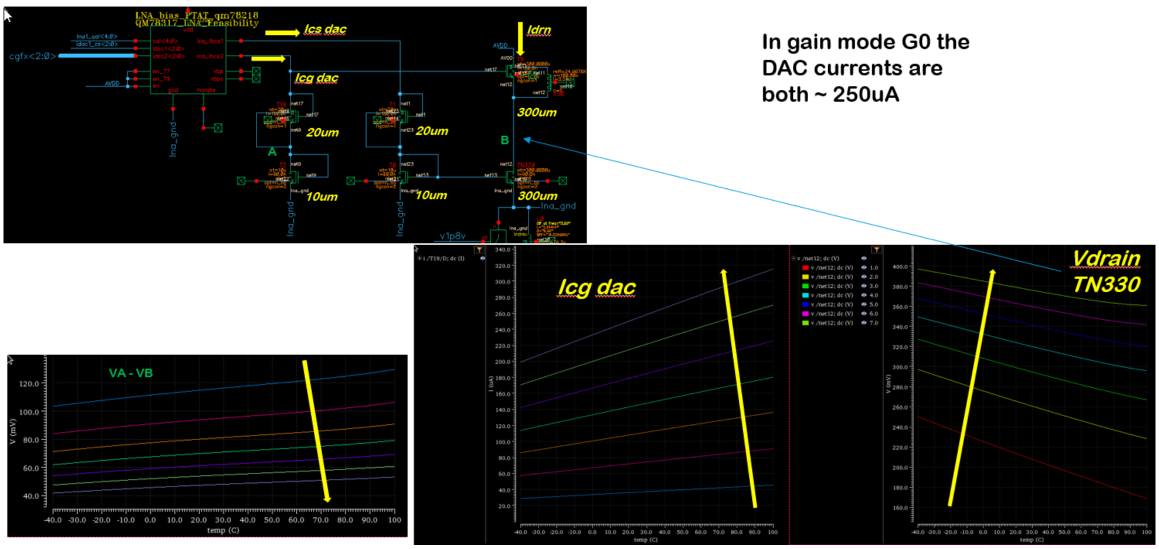

Figure 4

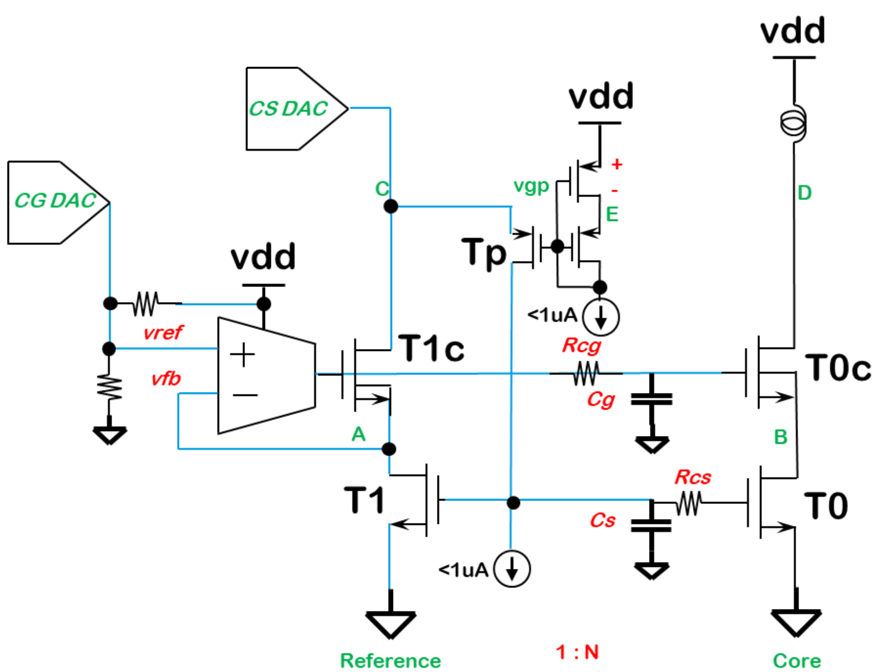

Figure 5a

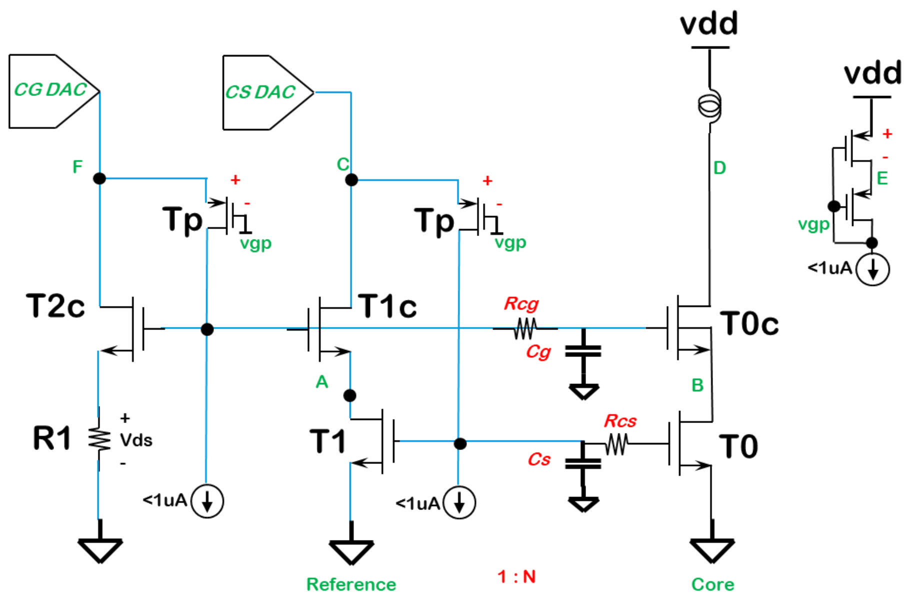

Figure 5b, 8b

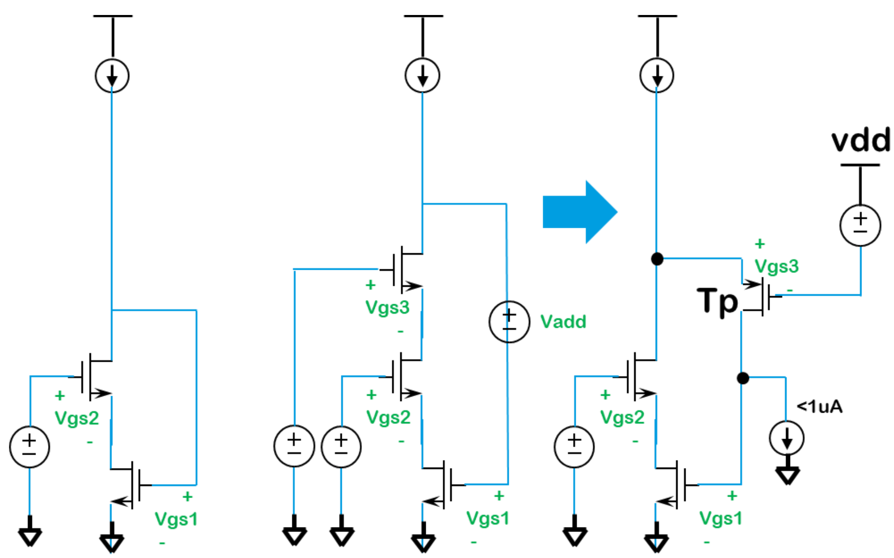

Figure 6a

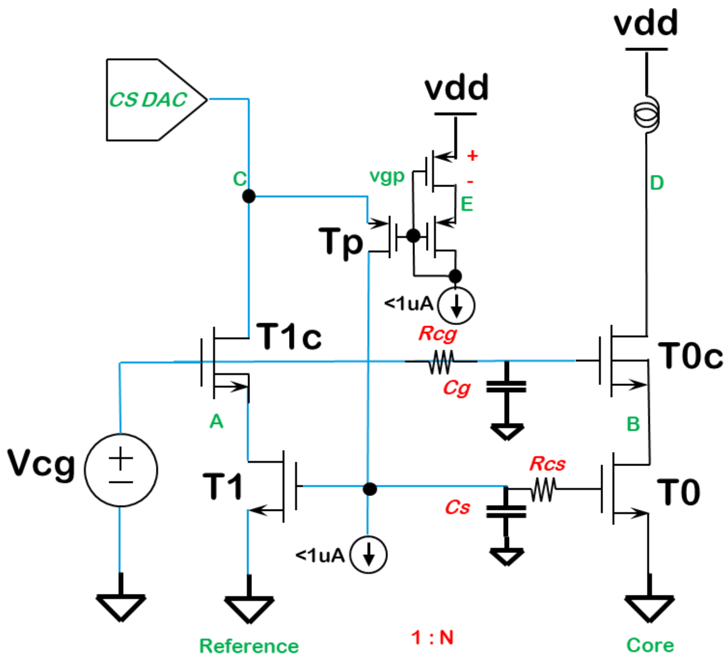

Figure 6b

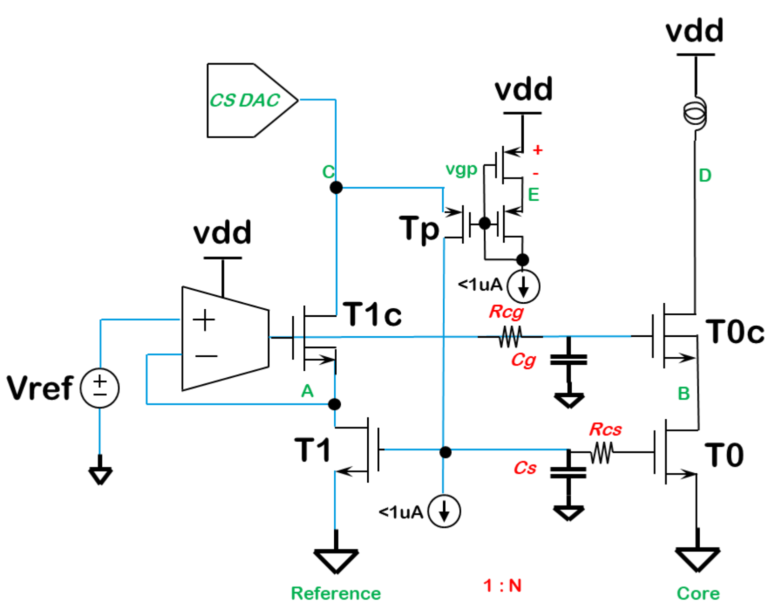

Figure 6c

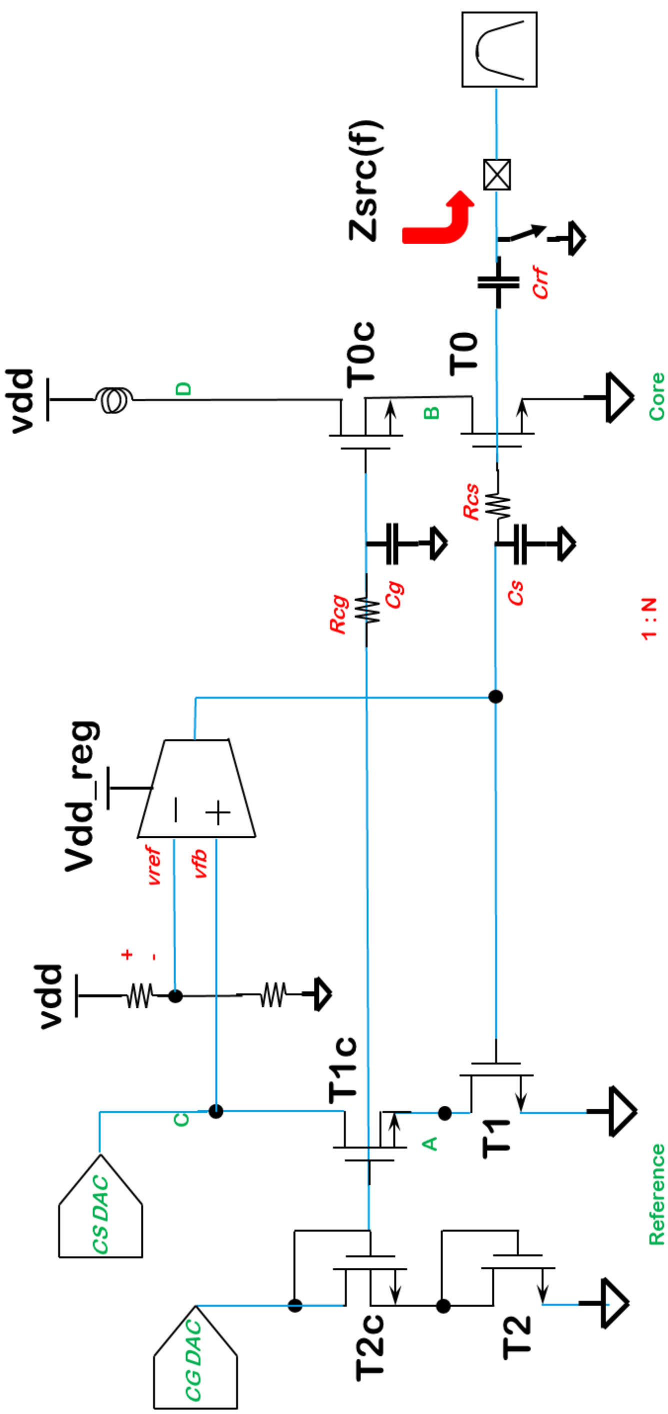
vdd
D
T0c
B
T0
Core
Zsrc(f)
Crf
Rcs
Rcg
Cg
Cs
1 : N
Vdd_reg
vref
vfb
+
-
vdd
T1c
C
A
T1
CS DAC
CG DAC
T2c
T2
Reference

Figure 7a

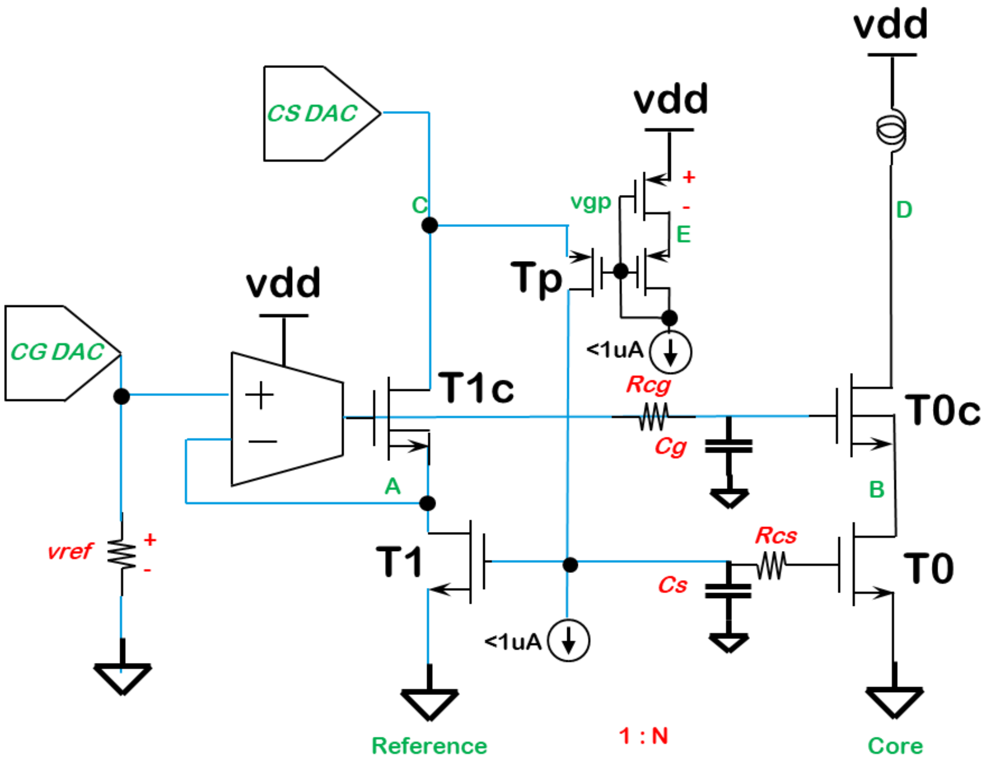
vdd
CS DAC
vdd
C
vgp
+
-
E
D
Tp
vdd
CG DAC
<1uA
T1c
Rcg
T0c
Cg
A
B
vref
+
-
Rcs
T1
T0
Cs
<1uA
Reference
1 : N
Core

Figure 8a