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## IMPROVING POINT OF LOAD EFFICIENCY BY DECREASING INDUCTOR SERIES RESISTANCE

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## IMPROVING POINT OF LOAD EFFICIENCY BY DECREASING INDUCTOR SERIES RESISTANCE

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### ABSTRACT

The manufacturers of electronic devices are constantly searching for efficiency improvements in point-of-load (POL) devices. To address that need, techniques are presented herein that support using low-cost graphite powder to improve inductor series resistance and conductivity. Under aspects of the presented techniques, multi-layer graphene may also be used to achieve significantly higher efficiency gains. It is anticipated that application of the presented techniques will yield a nominal gain of between 0.1% and 0.2%, which is significant when such a solution is applied to the many POLs that reside within a single design and across the millions of units that are sold.

### DETAILED DESCRIPTION

The manufacturers of electronic devices are constantly searching for efficiency improvements in point-of-load (POL) devices. In particular, in connection with manufacturer net zero initiatives (which seek a balance between the amount of greenhouse gas that is produced and the amount that is removed from the atmosphere) every possible improvement will benefit a manufacturer.

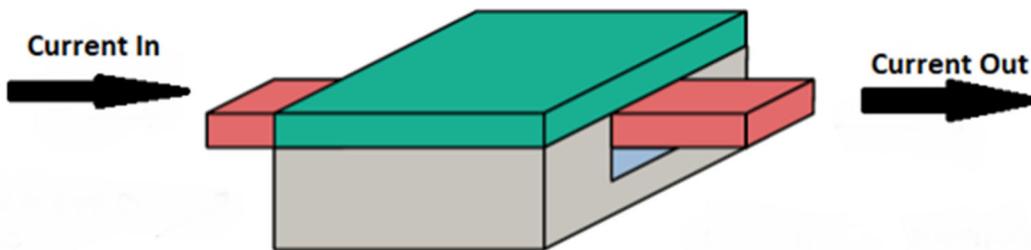
For example, the total system power efficiency in one network equipment vendor's new device suite is approximately 85% to 87%. Most of the low-hanging fruit to recover additional efficiencies has already been addressed in the use of integrated graphene in power planes, and in many other efforts that attempt to increase power efficiency.

Attaining the desired improvements that were referenced above is further complicated by application-specific integrated circuit (ASIC) designs which draw significant current in very small areas. In the recent past, ASIC power consumption was

less than 60 watts (W). Presently, it is surpassing 800W. With only a 0.6 volt (V) range for the rail, the massive amount of current that is required becomes clear.

To address the challenges that were described above, techniques are presented herein that support the application of graphite or graphene to the conductor that is passing through the magnetic structure comprising an inductor. Application of aspects of the presented techniques improve the efficiency of an inductor, particularly inductors that are used in POL devices.

Figure 1, below, presents a diagram illustrating elements of a wire inductor that may be constructed with a coated conductor according to aspects of the techniques presented herein.



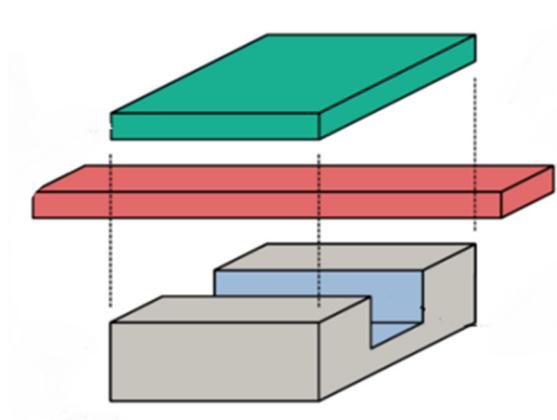
*Figure 1: Exemplary Wire Inductor – Assembled View*

As depicted in Figure 1, above, the wire inductor may comprise a two-piece ferrite core (identified by the colors teal and gray in the figure) through which passes a rectangular conductor (identified by the color light red in the figure). One end of the conductor may support an input terminus, the other end of the conductor may support an output terminus, and electric current may flow through the conductor.

According to aspects of the techniques presented herein, the indicated rectangular conductor may comprise fine graphite coated copper over plating. Alternatively, multi-layer graphene coated copper under surface plating may be employed. Additionally, a conductor may be coated with a fine graphite powder to realize a further improvement to conductivity.

A typical application for a wire inductor as depicted in Figure 1, above, is power delivery in a high-power POL design.

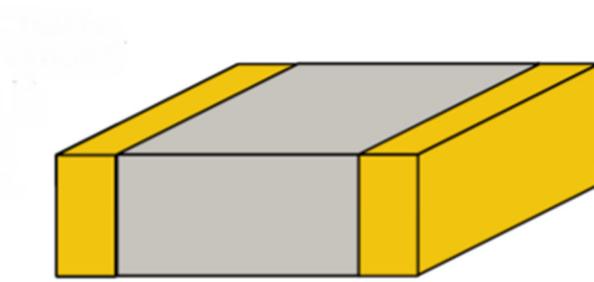
Figure 2, below, presents an exploded view of the wire inductor that was depicted in Figure 1, above, thus providing further details regarding aspects of the techniques presented herein.



*Figure 2: Exemplary Wire Inductor – Exploded View*

As depicted in Figure 2, above, the wire inductor may comprise a core that is composed of a composite ferro-magnetic material (which is identified by the color gray in the figure) and which includes a pass-through chamber. A graphite coated rectangular conductor (which is identified by the color light red in the figure) may reside in the pass-through chamber. A cover that is composed of the same composite ferro-magnetic material as described above (and which is identified by the color teal in the figure) may reside atop the core and may be secured with glue.

Figure 3, below, presents a diagram of a composite version of a ferrite bead inductor that is possible according to aspects of the techniques presented herein.

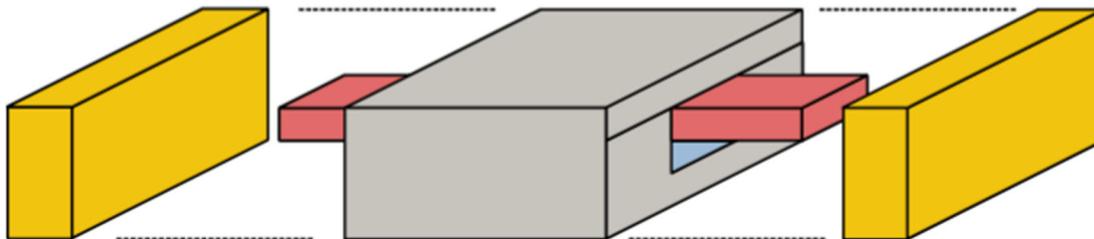


*Figure 3: Composite Ferrite Bead Inductor – Assembled View*

As depicted in Figure 3, above, the composite ferrite bead inductor may comprise a ferrite core (which is identified by the color gray in the figure) having, as will be shown in Figure 4, below, a pass-through chamber within which may reside a conductor. Two end caps (which are identified by the color yellow in the figure) may be affixed to the ends of the ferrite core, thus closing off the pass-through chamber.

A fully-assembled composite ferrite bead inductor, as illustrated in Figure 3, above, may, among other things, provide for a more efficient surface-mount technology (SMT) process or be helpful in small footprint applications. A typical application for such a composite ferrite bead inductor is electromagnetic compatibility (EMC) and/or electromagnetic interference (EMI) filtering and low-power applications to control interference.

Figure 4, below, presents an exploded view of the composite ferrite bead inductor that was depicted in Figure 3, above, thus providing further details regarding aspects of the techniques presented herein.



*Figure 4: Composite Ferrite Bead Inductor – Exploded View*

As depicted in Figure 4, above, the composite ferrite bead inductor may comprise a ferrite core (which is identified by the color gray in the figure) having a pass-through chamber within which may reside a conductor (which is identified by the color light red in the figure). Two end caps (which are identified by the color yellow in the figure) may be affixed to the ends of the ferrite core, thus closing off the pass-through chamber.

Depending upon the specific implementation, simulations have demonstrated that an improvement in inductor efficiency of between 0.03% to 0.25% may be achieved through the application of aspects of the techniques presented herein. Simulations have not demonstrated an improvement beyond 0.5%, thus that value is believed to be the

experimental maximum gain that may be achieved. Figure 5, below, presents a set of exemplary calculations regarding the efficiency improvements that were described above.

NOTE: FINE GRAPHITE WILL IMPACT SERIES RESISTANCE BY A 7.7%  
 USING GRAPHENE IN THE SAME STRUCTURE IS EXPECTED TO IMPACT SERIES RESISTANCE IN THE RANGE OF 20% TO 60% DEPENDENT ON LAYER STRUCTURE OF GRAPHENE LAYERS

$$\text{POWER (LOSS)} = I_{\text{RMS}}^2 * LRS$$

<p>USING GRAPHITE          ASSUME I = 10 AMPS</p> <p><math>R_{SDC} \approx .20 \text{ mohms}</math></p> <p><math>P = 100 * .00020</math>  <math>= 20 \text{ mW LOSS}</math>  <small>PWR PHASE PWR POL</small></p> <p><b>EFF GAIN = 0.033 %</b></p>	<p>NO ADDS</p> <p><math>R_{SDC} \approx .22 \text{ mohms}</math></p> <p><math>P = 100 * .00022</math>  <math>= 22 \text{ mW LOSS}</math>  <small>PWR PHASE PWR POL</small></p>
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USING MULTI-LAYER GRAPHENE  
 ASSUME I = 10 AMPS

$R_{SDC} \approx .15 \text{ mohms}$

$P = 100 * .00015$   
 $= 15 \text{ mW LOSS}$   
PWR PHASE PWR POL  
 USING 3 LAYERS GRAPHENE  
 AS SHOWN IN PREVIOUS COPPER  
 PLANE FILING.

**EFF GAIN = 0.117 %**

WE THINK THE IMPROVEMENT MAXIMIZES AT 0.25% BASED ON GRAPHENE COPPER PLANE ANALYSIS.

Figure 5: Exemplary Efficiency Improvement Calculations

It is anticipated that application of the presented techniques will yield a nominal gain of between 0.1% and 0.2%, which is significant when such a solution is applied to the many POLs that reside within a single design and across the millions of units that are sold.

Figure 6, below, depicts elements of an exemplary circuit incorporating inductors in a multi-phase power supply within a POL.

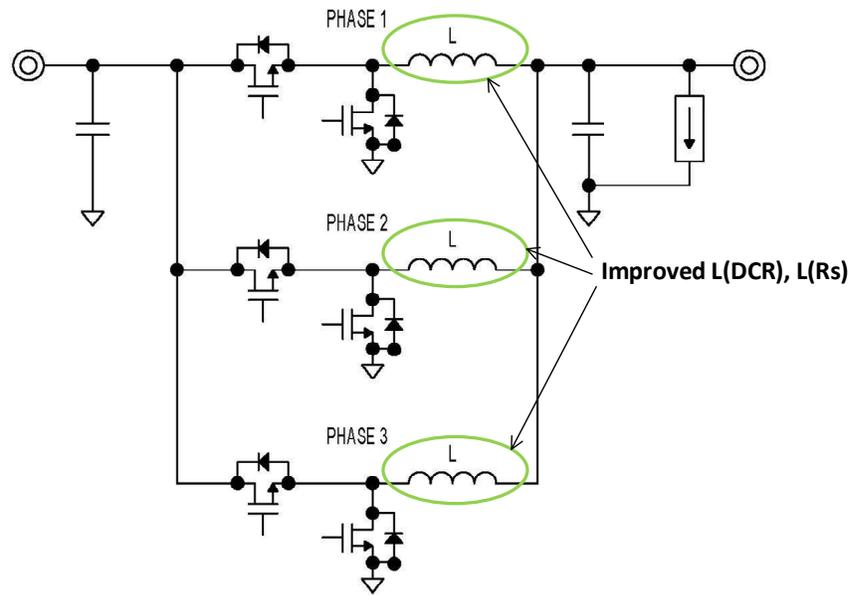


Figure 6: Exemplary Circuit

As illustrated in Figure 6, above, application of the techniques presented herein within the depicted circuit may yield improvements to inductor direct current (DC) resistance (DCR) (which is indicated as  $L(\text{DCR})$  in the figure) and to inductor loss (series) resistance ( $R_s$ ), which is indicated as  $L(R_s)$  in the figure.

In connection with the techniques presented herein, as described and illustrated in the above narrative, a number of important observations were made during an analysis and experimentation process. First, inductor  $R_s$  may be improved through the application of a graphite coating to a conductor. Further, inductor  $R_s$  may be decreased by approximately 10% through the use of graphite powder. Still further, a significant improvement (of almost 60%) in inductor  $R_s$  would be expected through the use of graphene integrated copper.

In summary, techniques have been presented herein that support using low-cost graphite powder to improve inductor series resistance and conductivity. Under aspects of the presented techniques, multi-layer graphene may also be used to achieve significantly higher efficiency gains. It is anticipated that application of the presented techniques will yield a nominal gain of between 0.1% and 0.2%, which is significant when such a solution is applied to the many POLs that reside within a single design and across the millions of units that are sold.