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Proxy Mode for Accessing Input/Output Pins in Multi-Dice Silicon Modules

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ABSTRACT

Multi-dice modules can be assembled on a package substrate with high precision and small dimensions, e.g., in micrometers. The package substrate may be a traditional organic substrate, or an advanced substrate such as a silicon interposer, silicon bridge, or 3D silicon stack. Once a multi-die module is assembled, certain edges of an individual die become difficult to access due to their close proximity to other dice. This disclosure describes techniques to address input/output (IO) port access in multi-die modules by utilizing other dice in the module as proxy IOs for a die with limited pin access. Input test patterns and output test results for a die-under-test with inaccessible ports are routed through another die with accessible ports and with lines of communication with the die-under-test.

KEYWORDS

- Application specific integrated circuit (ASIC)
- Automatic test pattern generation (ATPG)
- Design for test (DFT)
- Silicon interposer
- Multi-chip module (MCM)
- Chiplet
- Die-to-die (D2D)
- Test compression
- Scan chain
- Scan chain compression

BACKGROUND

Application specific integrated circuits (ASICs) are evolving from single, monolithic silicon dice to heterogeneous multi-die modules. These multi-die modules are typically assembled on a package substrate or silicon interposer with very high precision and very small dimensions, e.g., in micrometers. The package substrate may be a traditional organic substrate, or an advanced substrate such as a silicon interposer, silicon bridge, or 3D silicon stack.

Once a multi-die module is assembled, certain edges of an individual die become difficult to access due to their close proximity to other dice. This leads to problems when performing manufacturing tests such as DFT (design for test) or ATPG (automatic test pattern generation). Die edges, also known as beachfronts, available during single die manufacture may no longer be available once the multi-die module is assembled. ASIC input/output (IO) ports, generally placed along die edges, can become inaccessible upon assembly. IO ports are used by DFT to provide ATPG patterns to the ASIC to test and screen for manufacturing defects. Reduced DFT access in the final packaged module leads to reduced test coverage, potentially resulting in undetected silicon faults or poor yield.

DESCRIPTION

This disclosure describes techniques that improve input/output (IO) port access in multi-chip (or multi-die) modules by utilizing other dice in the module as proxy IOs for a die with limited pin access.

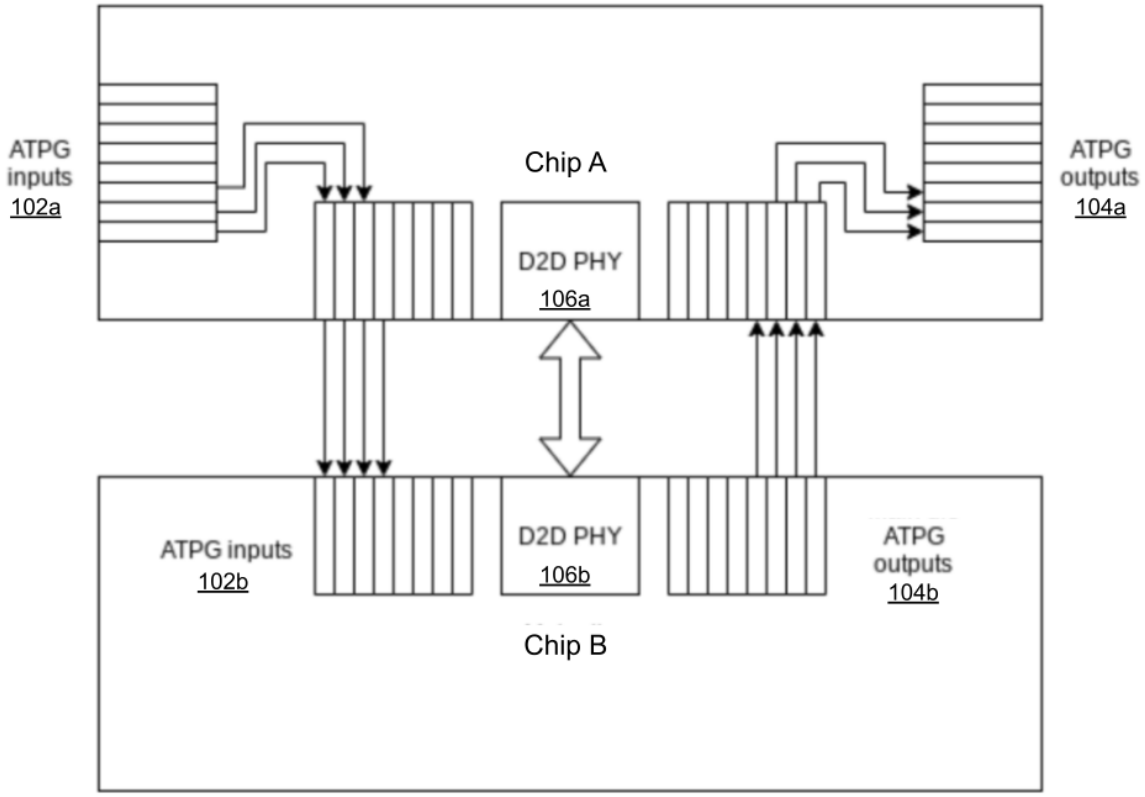

Fig. 1: Accessing input/output pins in multi-die silicon

Fig. 1 illustrates an example of accessing input/output pins in multi-die silicon. In this example, the ATPG inputs and outputs of chip B (which can be a main die) are inaccessible once assembled alongside chip A (which can be a chiplet, or another main die). To make the IO pins of chip B accessible, chip A that has accessible input and output pins, is utilized to transport ATPG inputs (102b) into, and ATPG outputs (104b) out of chip B, thereby providing access to the IOs of chip B even after the multi-die module has been assembled. ATPG inputs designed for chip B are provided at the input pins of chip A (102a), and, after exercising chip B, outputs are tapped at the output pins of chip A (104a). Flip-flop cells can be added to chip A to achieve accurate timing of high-speed signals that travel between chips A and B. ATPG patterns developed for standalone testing of chip B can advantageously be ported to the multi-die package

with no changes to the test patterns, resulting in identical test coverage during standalone and multi-die package testing.

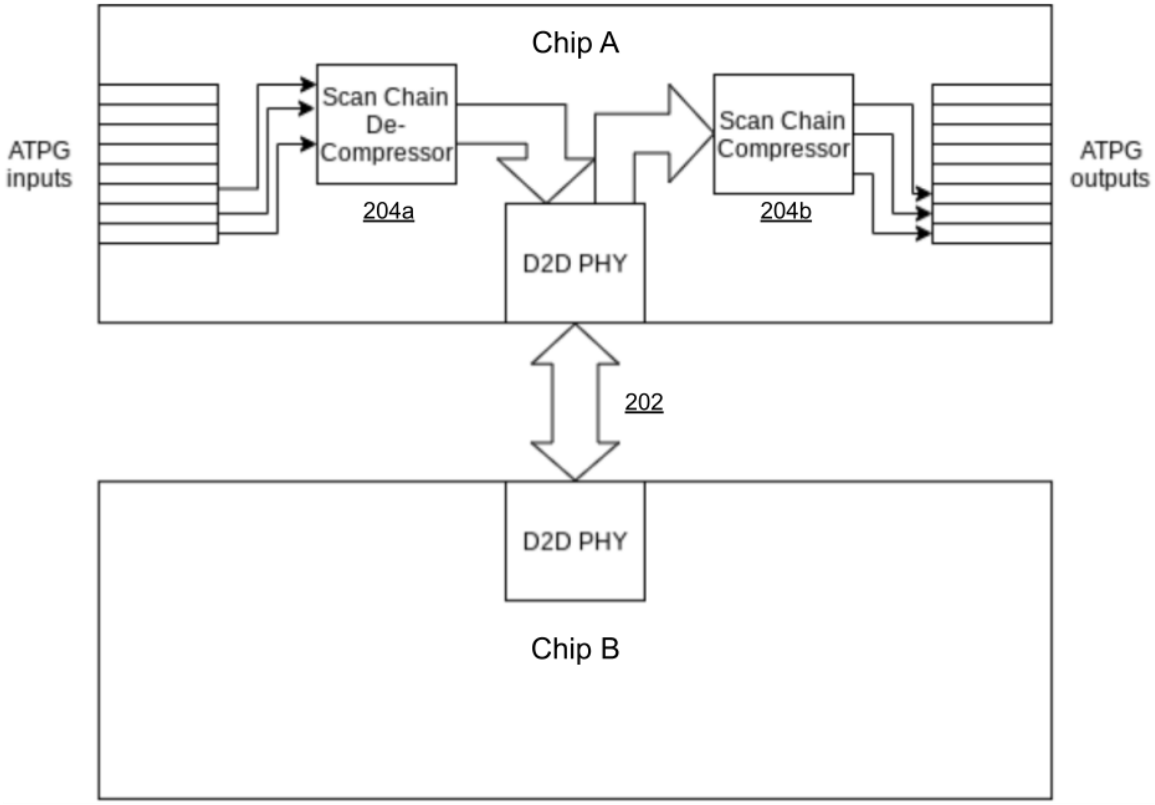

Fig. 2: Accessing input/output pins in multi-die silicon via the D2D PHY layer

Fig. 2 illustrates another example of accessing IO pins in multi-die silicon. In this example, the die-to-die (D2D) PHY (202), which is a high-speed serial communication interface between chips, is used to carry ATPG signals. As before, ATPG signals that target chip B (which can be a main chip) are routed through chip A (which can be a chiplet or another main die). Chip A includes scan-chain de-compressor (204a) and compressor (204b) modules. Scan chain compressors can create, e.g., 10:1 or more scan chain copies from one IO interface. A D2D interface typically has thousands of signals or more. Alternatively, the D2D PHY may utilize high-speed transmission techniques such as a Serializer/Deserializer (SerDes) interface.

Uncompressed scan chains are transported into chip B via the D2D PHY. The output (test result) of chip B is transported via the D2D PHY to chip A, where it is processed by the scan-chain compressor to obtain the ATPG outputs of chip B. In this example, ATPG patterns developed for standalone testing of chip B can be different from the patterns developed for the final multi-die package. However, there is no real reduction in test pattern coverage.

CONCLUSION

This disclosure describes techniques to address input/output (IO) port access in multi-die modules by utilizing other dice in the module as proxy IOs for a die with limited pin access. Input test patterns and output test results for a die-under-test with inaccessible ports are routed through another die with accessible ports and with lines of communication with the die-under-test.