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March 2022

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Recommended Citation

Nozadze, David; Koul, Amendra; Sapozhnikov, Mike; Kareti, Upen Reddy; and Goergen, Joel, "PREDICTION OF POST-FEC PERFORMANCE WITHOUT USING FEC SYMBOLS COUNTERS", Technical Disclosure Commons, (March 15, 2022)

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PREDICTION OF POST-FEC PERFORMANCE WITHOUT USING FEC SYMBOLS COUNTERS

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ABSTRACT

Some application-specific integrated circuits (ASICs) do not have counters for forward error correction (FEC) symbol errors so it is not possible to predict a post-FEC bit error rate (BER) when a pre-FEC BER is small (e.g., less than $1E-5$). Without FEC statistics, it is not possible to predict a post-FEC BER. To address such a challenge, techniques are presented herein that support a method for predicting post-FEC performance without requiring counters for FEC symbol errors. Aspects of the presented techniques implement a mathematical model which calculates and predicts a post-FEC BER for a given pre-FEC BER. Such a predicted post-FEC BER may subsequently be utilized to develop a frame loss ratio (FLR) and a codewords error ratio (CER).

DETAILED DESCRIPTION

In some cases (e.g., in some application-specific integrated circuits (ASICs) that are employed within different network equipment vendors) the physical retimers that are employed do not have counters for forward error correction (FEC) symbol errors so it is not possible to predict a post-FEC bit error rate (BER) when a pre-FEC BER is small (e.g., less than $1E-5$). Without FEC statistics, it is not possible to predict a post-FEC BER.

To address the type of challenge that was described above, techniques are presented herein that support a method to predict post-FEC performance without requiring counters for FEC symbol errors. Aspects of the presented techniques implement a mathematical model which calculates and predicts a post-FEC BER for a given pre-FEC BER. The model takes into account error propagations and correlations including ASIC process (P) corners, sweep voltage (V) or power noise, and temperature (T) (i.e., PVT); insertion loss (IL); and crosstalk (xtalk) dependency. For different PVT variations, IL values, and xtalk

levels, a post-FEC BER versus a pre-FEC BER for a high pre-FEC BER may be collected so that a post-FEC BER may be developed. Such a measurement may be fit to the model and then extrapolated to predict a post-FEC BER.

Figure 1, below, depicts elements of a process flow according to aspects of the techniques presented herein and reflective of the above discussion.

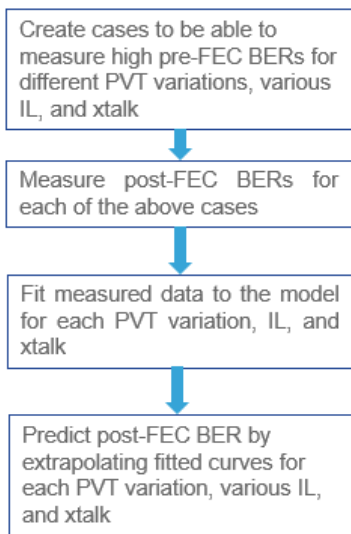


Figure 1: Exemplary Post-FEC BER Prediction Flow

As described above, aspects of the techniques presented herein support a post-FEC BER prediction model through which a post-FEC BER value may be developed for a given pre-FEC BER. Among other things, the model takes into account error propagations and correlations. Additionally, the model is analytical. Under the model, a post-FEC BER versus a pre-FEC BER may be measured for a high pre-FEC BER (e.g., $1E-6$ to $1E-4$), fit to the model, and then extrapolated to predict a post-FEC BER.

Figure 2, below, presents a set of illustrative curve tracings (where an indicated *er_prp* curve measures the strength of different error propagations and correlations, with a larger value indicating higher error propagations and correlations) that are reflective of the above discussion.

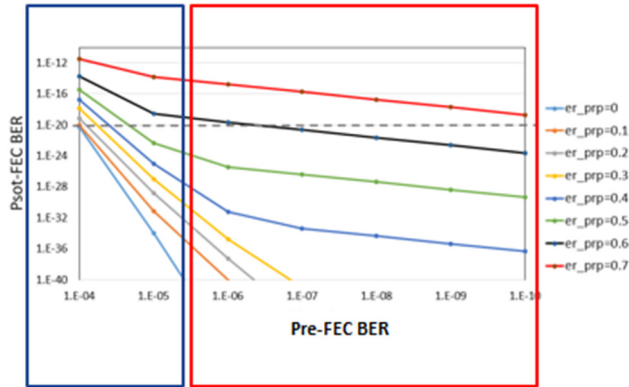


Figure 2: Illustrative Curve Tracings

Through the blue left-hand side and the red right-hand side of Figure 2, above, measured data may be fit to any of the depicted curves to read out an extrapolated post-FEC BER for a good pre-FEC BER.

It is important to note that the prediction model that was described above, that is available through the techniques presented herein, encompasses the estimation of a post-FEC BER with and without burstiness. Figure 3, below, depicts elements of a burst example. E.N. Gilbert, *Capacity of a Burst-Noise Channel*, Bell Systems Technical Journal, Vol. 39, pp. 1253-1265, 1960.

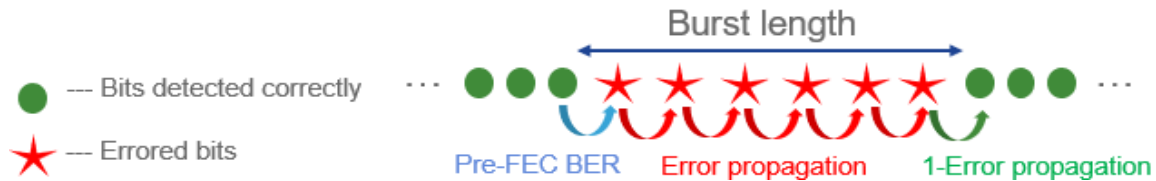


Figure 3: Illustrative Burst Example

As depicted in Figure 3, above, a post-FEC BER is degraded as error propagation probability increases.

According to aspects of the techniques presented herein, the methodology for the above narrative encompasses the capture of V, T, IL, and xtalk levels for each ASIC P corner and the measurement of a pre-FEC and a post-FEC BER. Such measurements may be taken at different time periods (e.g., three iterations of one-hour increments) to monitor how a post-FEC BER is varying and ensure that it is saturated and not changing.

For each of the above data points a post-FEC BER versus a pre-FEC BER may be fit to the above-described model through the curve tracings that were presented in Figure 2, above. Such an approach will provide an error propagation factor for each case. Thus, the error propagation factor will be a matrix or function $er_prp(V, T, IL, xtalk, P)$.

The methodology that was described above may be applied to a number of real-world systems to, for example, predict or measure IL and T, read out a P corner and V, and quantify an xtalk level. Using the above information, it is possible to look up an er_prp factor (based on the calculations that were previously described). With the knowledge of an er_prp factor and a pre-FEC BER in a real system it is possible to predict a post-FEC BER using the above-described model through extrapolation.

A post-FEC BER that is developed according to aspects of the techniques presented herein may subsequently be utilized to develop a frame loss ratio (FLR) and a codewords error ratio (CER). In particular, a CER (e.g., for a Reed Solomon RS(544) FEC) may be calculated through the following formula (Pete Anslow, *RS(544,514) FEC Performance for KR/CR 100G (updated)*, IEEE P802.3ck Task Force, Apr. 10, 2019, https://iee802.org/3/ck/public/adhoc/apr10_19/anslow_3ck_adhoc_01_041019.pdf):

$$CER = \sum_{i=16}^{544} CER_i$$

For the formula above, the term CER_i is the probability of having codewords with i number of symbols errors. As $CER_{16} \gg CER_{i>16}$ it is possible to obtain the relationship $CER \approx CER_{16}$. Then:

$$CER = \frac{Post-FEC\ BER * 5440}{16}$$

Since a FLR and a CER are approximately same, a FLR may be calculated using the above equations.

As described and illustrated above, the techniques presented herein support a means for predicting, without knowing any statistics regarding FEC symbol errors, a post-FEC BER, a FLR, and a CER for different PVT variations, IL values, and xtalk levels.

While the model that was described above is based on a one-tap decision feedback equalization (DFE), it may be generalized to multiple DFE taps using, for example, Monte Carlo simulations. Additionally, the methodology that was described above is not limited to just a RS(544) FEC but may be applied to other FECs.

Existing solutions that attempt to predict a post-FEC BER using a pre-FEC BER (or other metrics) do not take into account FEC burst errors or use corrected FEC symbols counter statistics to predict post-FEC behavior while taking FEC burstiness into account. Accordingly, those solutions are not applicable in a case where there are FEC burst errors and FEC counters are not available. In real life, burst errors in a FEC are almost always present and typically arise due to PVT variations, channel reflections, xtalk, or Serializer/Deserializer (SerDes) transmit (TX) or receive (RX) jitter and equalizations.

In contrast, aspects of the techniques presented herein are able to predict a post-FEC BER, without requiring FEC counters, using a pre-FEC BER, assuming burst errors are present, and taking into account PVT variations, channel reflections, xtalk, or SerDes TX or RX jitter and equalizations. All of those perturbations may cause burst errors and can dramatically impact the accuracy of a post-FEC BER prediction if some other method is not used which account for burstiness. Such a method is found in the techniques presented herein through the fitting model that was described above.

In summary, techniques have been presented that support a method for predicting post-FEC performance without requiring counters for FEC symbol errors. Aspects of the presented techniques implement a mathematical model which calculates and predicts a post-FEC BER for a given pre-FEC BER. Such a predicted post-FEC BER may subsequently be utilized to develop a FLR and a CER.