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L2VPN Pseudowire status notification in BGP-AD VPLS Environment

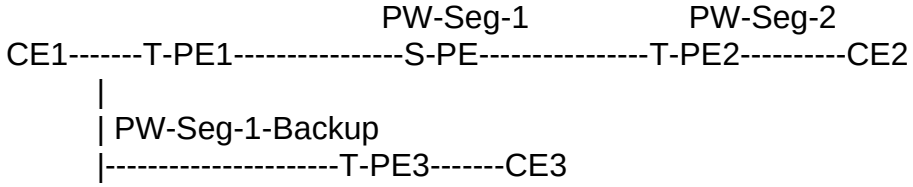
ABSTRACT

PW status signaling is common in dynamic PWs established through T-LDP signaling, but there is no mechanism to signal the status of PW (and various associated faults) in BGP signaled PW in BGP-AD VPLS environment. In hybrid multi-segmented environments e.g. in hierarchical networks where the ownership of different segments of the NW, and hence underlying signaling methods, lies with different operators and/or administrators, end-to-end fault signaling becomes problematic). It is propose that L2VPN Pseudowire status can be sent for BGP-AD VPLS signaled pseudowires as a solution for this problem.

DETAILED DESCRIPTION

Problem Statement:

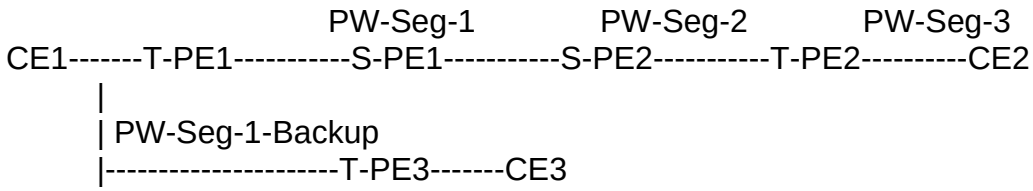
Consider the below scenarios:



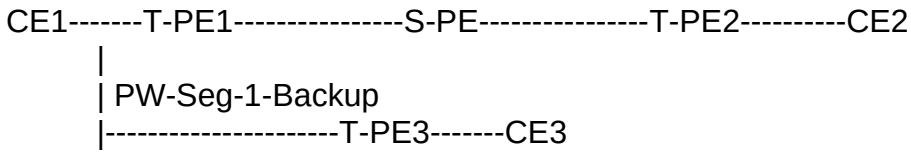
Here, Multi-Segment Pseudowire has been established between T-PE1- and T-PE2 with S-PE node acting as switching PE. PW-seg-1 is established through targeted LDP (Label Distribution protocol) and PW-seg-2 is established through BGP-AD VPLS (Refer below for acronyms). PW-seg-1-Backup is backup pw of PW-seg-1. Here, STLV is enabled inside TLDP so that if any PW fault occurs in segment-1 or segment-2, the fault would be notified to T-PE1 through STLV, and Pw switchover will happen to backup PW. PW-Seg-1-Backup at T-PE1 and traffic will resume.

The problem comes when the AC between T-PE2 and CE2 goes down. There is no way in BGP-AD VPLS to signal the AC fault as PW status. So, the PW switchover will not happen on T-PE1 and the traffic from CE1 will keep on flowing till T-PE2 where it will get blackholed.

Other Scenarios where the same problem would be seen:



Here, everything is same as in the first scenario, but PW-Seg-1 is established using TLDP, PW-Seg-2 is established using BGP-AD-VPLS and PW-Seg-3 is established using TLDP.



Here, the only difference with the first scenario is that PW-Seg-1 is static instead of dynamic PW. So, this is a case of hybrid MS-PW. There may be some other scenarios in hybrid segmented networks where this problem and the proposed solution applies.

Solution Offered:

This disclosure introduces a method to send PW status inside BGP update message for BGP-AD VPLS PWs, so that the AC fault status can be sent to T-PE1, and PW switchover can happen on T-PE1.

Acronyms:

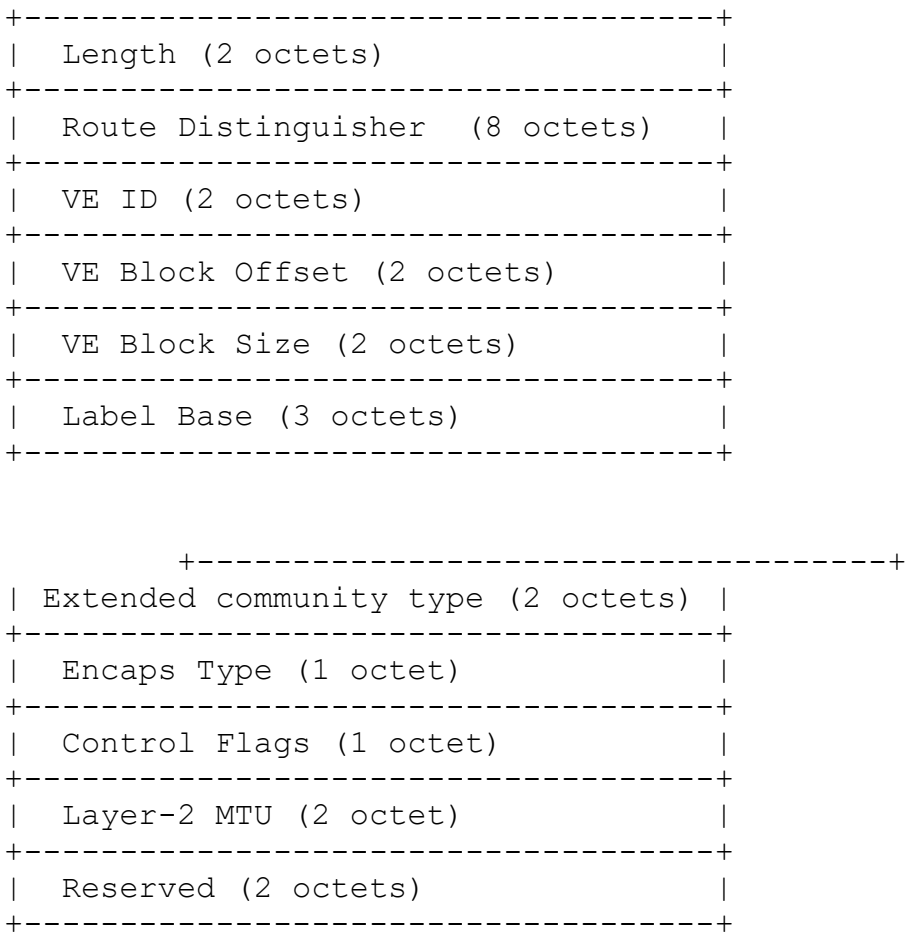
AC- Attachment Circuit
AD- Auto Discovery
BGP- Border Gateway Protocol
CE- Customer Edge
LDP- Label Distribution Protocol
L2VPN- Layer 2 Virtual Private Network
MS-PW- Multi Segment Pseudowire
PE- Provider Edge
PW- Pseudowire
STLV- Status Type Length Value
TLDP- Targeted LDP
VPLS- Virtual Private LAN Service

Novelty1: L2VPN PW status is sent inside BGP update message so that PW status can be propagated between PW end points.

Novelty2: PW protection switching is supported for protected BGP-AD VPLS PWs also, based on PW status sent in BGP update message.

The invention implements:
L2VPN Pseudowire status can be sent for BGP-AD VPLS signaled pseudowires.

“BGP VPLS NLRI” and “Layer2 Info Extended Community” are sent in below format inside BGP update message while establishing BGP-AD VPLS PWs.



Below is the approach to send PW status.

A new Path Attribute can be added to carry the PW status.

Path Attribute – PSEUDOWIRE_STATUS

Flags: 1 octet with the following fields

Optional(1 bit): Set

Transitive(1 bit): Set

Partial(1 bit): Not Set

Extended-Length(1 bit): Not Set

Unused(4 bits): 0000

Type Code: PSEUDOWIRE_STATUS(41)

Length: 16

Pseudowire Status(32 bits):

0x00000000 - Pseudowire forwarding (clear all failures)

0x00000001 - Pseudowire Not Forwarding

0x00000002 - Local Attachment Circuit (ingress) Receive Fault

0x00000004 - Local Attachment Circuit (egress) Transmit Fault

0x00000008 - Local PSN-facing PW (ingress) Receive Fault

0x00000010 - Local PSN-facing PW (egress) Transmit Fault

When the Pseudowire is signaled 1st time, the initial PW status would go in the BGP update message.

Subsequent triggered AC fault or Tunnel fault will also be sent using the above status codes in the BGP update message.

It will be appreciated that some embodiments described herein may include one or more generic or specialized processors (“one or more processors”) such as microprocessors, digital signal processors, customized processors, and Field-Programmable Gate Arrays (FPGAs) and unique stored program instructions (including both software and firmware) that control the one or more processors to implement, in conjunction with certain non-processor circuits, some, most, or all of the functions of the methods and/or systems described herein. Alternatively, some or all functions may be implemented by a state machine that has no stored program instructions, or in one or more Application-Specific Integrated Circuits (ASICs), in which each function or some combinations of certain of the functions are implemented as custom logic. Of course, a combination of the aforementioned approaches may be used. Moreover, some embodiments may be implemented as a non-transitory computer-readable storage medium having computer-readable code stored thereon for programming a computer, server, appliance, device, etc. each of which may include a processor to perform methods as described and claimed herein. Examples of such computer-readable storage mediums include, but are not limited to, a hard disk, an optical storage device, a magnetic storage device, a ROM (Read Only Memory), a PROM (Programmable Read-Only Memory), an EPROM (Erasable Programmable Read-Only Memory), an EEPROM (Electrically Erasable Programmable Read-Only Memory), Flash memory, and the like. When stored in the non-transitory computer-readable medium, the software can include instructions executable by a processor that, in response to such execution, cause a processor or any other circuitry to perform a set of operations, steps, methods, processes, algorithms, etc.

Although the present disclosure has been illustrated and described herein with reference to preferred embodiments and specific examples thereof, it will be readily apparent to those of ordinary skill in the art that other embodiments and examples may perform similar functions and/or achieve like results. All such equivalent embodiments and examples are within the spirit and scope of the present disclosure.