February 2022

Integrated, Switched-Capacitor Voltage Regulator with Deep-Trench Capacitor

N/A

Integrated, Switched-Capacitor Voltage Regulator with Deep-Trench Capacitor

ABSTRACT

Currently, switching regulators come with inductors that are by nature bulky and difficult to fit in or integrate with ASICs due to space and layout considerations. This disclosure describes a voltage regulator based on switched capacitors (SC) that eliminates external inductors, enabling the integration of the voltage regulator with the package and/or the die. Integrated voltage regulators are valued in ASIC packaging designs as they better support power-integrity challenges brought on by advanced computing and memory-bandwidth demands. The techniques leverage the presence of parasitic inductance present in the package or/and MLCC, rather than employ external inductances.

KEYWORDS

- Voltage regulator
- Switched capacitor
- Deep-trench capacitor (DTC)
- Integrated voltage regulator
- Integrated voltage regulator (IVR)
- Multilayer ceramic capacitor (MLCC)
- Parasitic inductance
- Active capacitor
- Power distribution network (PDN)
- Voltage controlled current source

BACKGROUND

Currently, switching regulators come with inductors that are by nature bulky and difficult to fit in or integrate with application-specific integrated circuits (ASICs) due to space limitations and layout considerations. Integrated voltage regulators are valued in ASIC packaging designs as they better support power-integrity challenges brought on by advanced computing and memory-bandwidth demands.

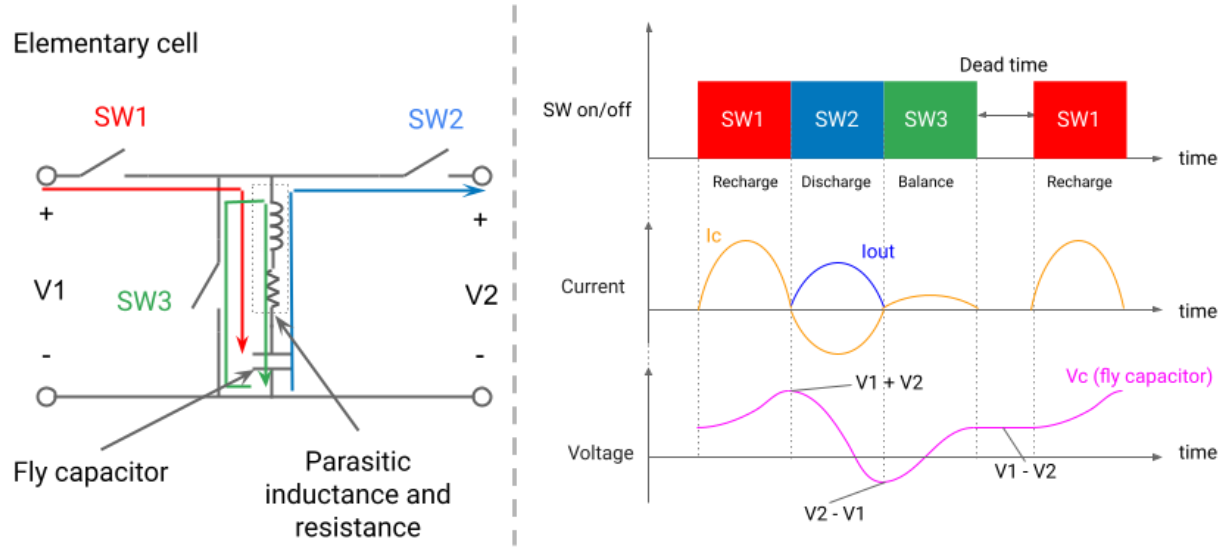
Current techniques [1, 2] that attempt fully integrated switched capacitors consider only on-die capacitances (MIM and MOS), which make the voltage regulator large and somewhat impractical. Also, the efficiency of current techniques depends on the topology, e.g., they are good only for fixed-ratio voltage conversion. Configurable topologies for different conversion ratios have resulted in complex and unpromising designs. Another approach, the resonant SC converter [3], addresses the efficiency issue under variant conversion ratios. However, its power density is low, and its use of an external inductor for integrated voltage regulation (IVR) is suboptimal.

DESCRIPTION

This disclosure describes a voltage regulator based on switched capacitors (SC) that eliminates external inductors, enabling the integration of a voltage regulator with the package and/or the die. The techniques leverage deep-trench capacitors (DTC) technology, which, by providing much more capacitance density compared to on-die intrinsic and metal-insulator-metal (MIM) capacitance, enables fully integrated SC in medium and large ASICs/CPUs. The techniques leverage the presence of parasitic inductance present in the package or/and multilayer ceramic capacitors (MLCC), rather than employ external inductances.

The described voltage regulator with integrated, switched, deep-trench or packaged MLCC capacitors includes switched-capacitor converter bricks/cells; digital control and clock generator; capacitors; etc. As described in greater detail below, the current/charges flow from input to fly capacitors through MOSFETs in the converter bricks/cells, then flow to output capacitors. Parasitic inductance in the path can help create an LC-resonance, so as to create a voltage-controlled current source. The frequency or dead time of MOSFETs switching is

controlled by the clock generator such that the output voltage across the output capacitor is at the desired level.



(a) **(b)**

Fig. 1: Integrated, switched-capacitor voltage regulator with DTC: (a) topology; (b) operation

Fig. 1(a) illustrates the topology of an elementary cell of the integrated, switched-capacitor voltage regulator with DTC, while Fig. 1(b) illustrates its operation. In Fig. 1(a), V1 is the input voltage and V2 is the output voltage. As illustrated, the deep-trench capacitor can be installed in flying mode. No external inductances or resistances are required. Rather, parasitic inductances and resistances of the DTC are leveraged to create a resonant circuit.

The switches SW1, SW2, and SW3 (which can each be field-effect transistors, FETs, or MOSFETs) open and close out-of-phase and in sequence, such that at any time, at most only one of the three switches is closed. In addition, there is a dead time when all three switches are open. The flow of current when a given switch is closed is indicated by the arrow of the corresponding color. For example, when SW1 closes, the capacitor (re-)charges through the input, indicated by the red arrow. When SW2 closes, the capacitor discharges through the output, indicated by the

blue arrow. When SW3 closes, the capacitor reaches a state of balance, e.g., a current (green) flows through the L-C circuit made of the capacitor and the parasitic inductance. When all three switches are open (dead time), no current flows aside from leakage currents, e.g., the fly capacitor voltage remains constant. The time duration of SW1, SW2 and SW3 should be controlled to $\pi\sqrt{LC}$ so that the transition between SW1 to SW2, or SW2 to SW3 happens at zero current and all energies are stored at the capacitor and ideally there is no power loss.

A major advantage of using this topology as the basic cell, not observed in previous studies, is that no matter how many cells are stacked or any timing difference that exists, the circuit resonance frequency - $2\pi\sqrt{LC}$ - remains the same, presuming output and input inductance is negligible. Therefore, power density can be accumulated simply by stacking more cells while the overall structure remains simple.

Fig. 1(b) illustrates the currents through the capacitor (Ic, yellow) and the output (Iout, blue), and the voltage (Vc, pink) across the fly capacitor over the recharge-discharge-balance-dead-time cycle of the voltage regulator.

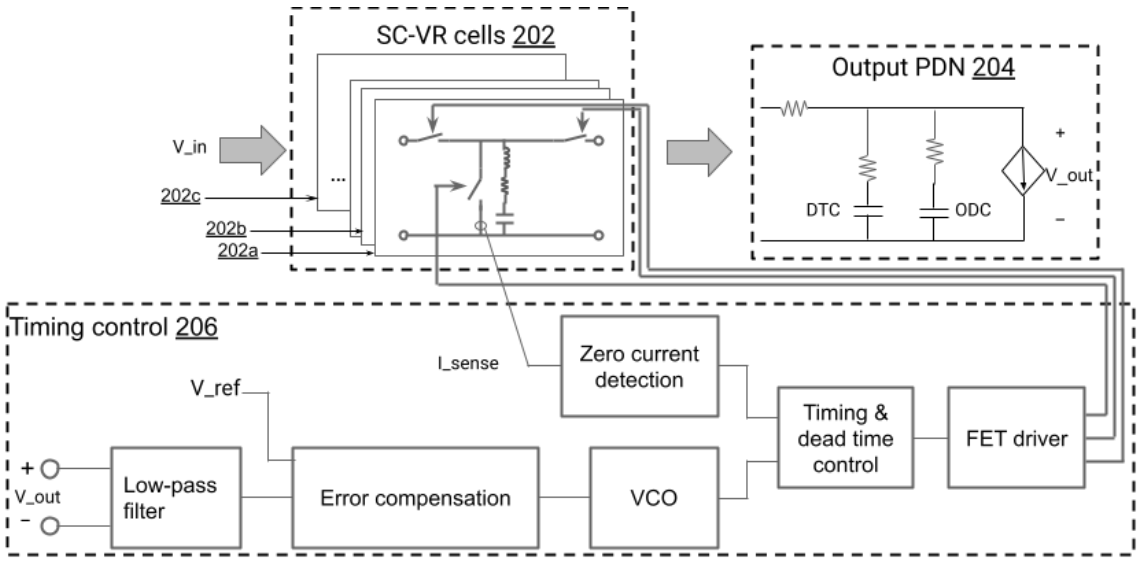


Fig. 2: Developing a greater power output by arranging VR cells in parallel and by sequencing their operations

Fig. 2 illustrates developing a greater power output by arranging a battery of switched-capacitor VR cells (202) in parallel and by sequencing their operations. As illustrated, the battery of switched-capacitor VR cells comprises elementary SC-VR cells (202a-c) of the type illustrated in Fig. 1a, such that their sum current feeds into an output power distribution network (PDN 204).

The component switches of each elementary SC-VR cell are driven by a timing control circuit (206) such that the output currents (Iout) of each elementary cell are slightly offset in time from each other. In this manner, as illustrated in Fig. 3, a battery of elementary SC-VR cells can deliver a nearly constant current to a load. Timing control is achieved by comparing the time-filtered output voltage (V_out) to a reference voltage (V_ref) and by using the resulting error signal to adjust the relative firing timings and the dead times of the elementary SC-VR cells. Zero current detection is used to set the correct duration of SW1-3.

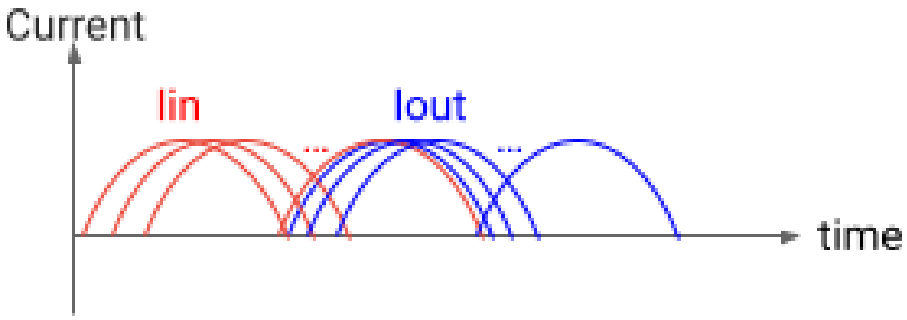


Fig. 3: A battery of elementary SC-VR cells delivers a nearly constant output current (Iout)

As illustrated in Fig. 3, the output currents (Iout, blue) of a number of elementary SC-VR cells comprising the battery are timed to be slightly out of phase, such that their sum current delivered to the load is nearly constant.

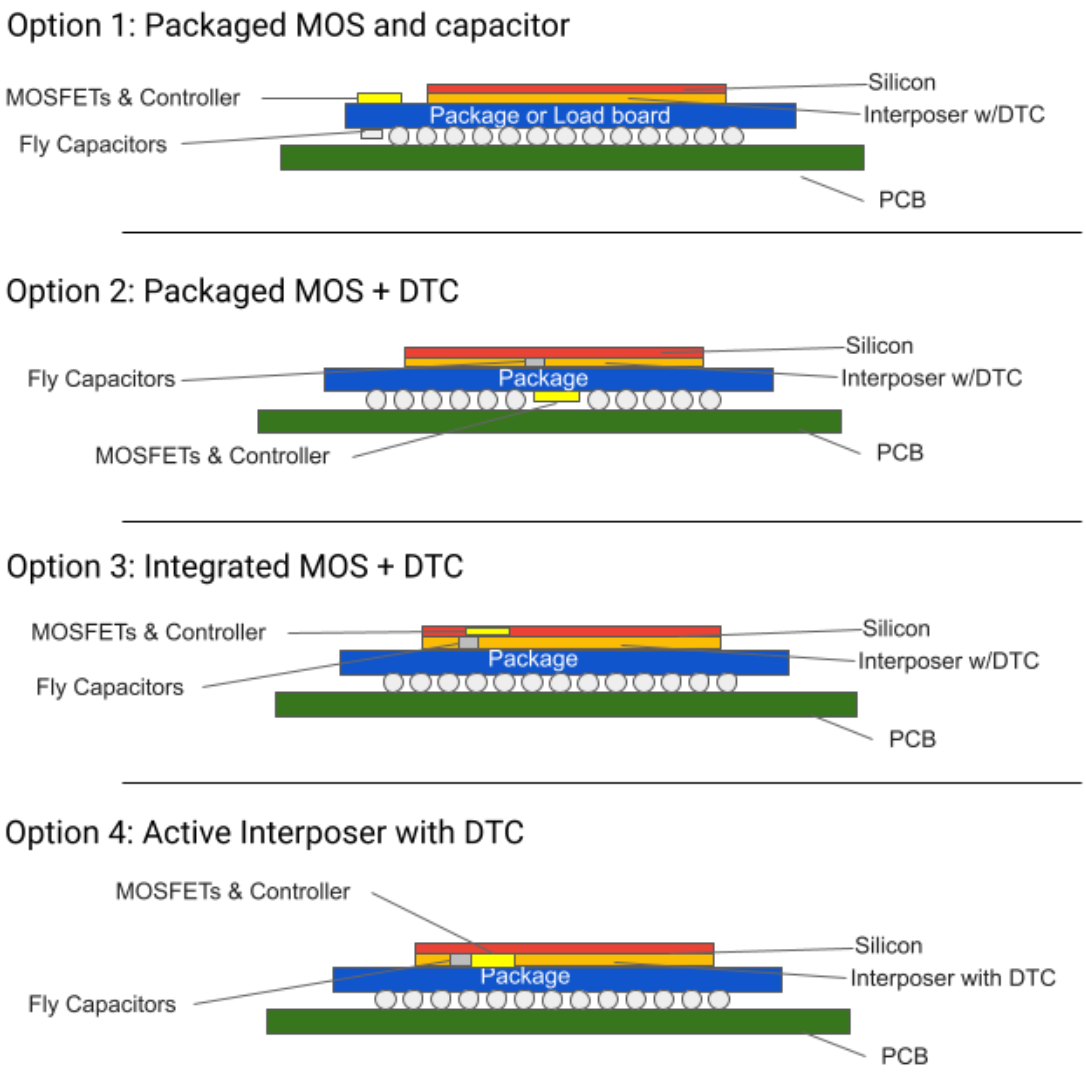


Fig. 4: Packaging and integration options

As illustrated in Fig. 4, a variety of options exist for packaging and integrating the described switched-capacitor voltage regulator into an ASIC or die. For example, in option 1, the MOSFETs, controller, and fly capacitors can be installed on the package (load) board. In option 2, the fly capacitors are on the interposer while the MOSFETs and controller are on the package. In option 3, the MOSFETs and controller are in the silicon while the fly capacitors are in the interposer. In option 4, the MOSFETs, controller, and the fly capacitors are in the interposer, making it an active interposer.

In this manner, by leveraging parasitic inductance in deep-trench capacitors, a compact, switched-capacitor voltage regulator can be tightly integrated with ASICs to conserve space. Since the parasitic inductors have low resistance, higher switching bandwidth and efficiency can be achieved.

CONCLUSION

This disclosure describes a voltage regulator based on switched capacitors (SC) that eliminates external inductors, enabling the integration of the voltage regulator with the package and/or the die. Integrated voltage regulators are valued in ASIC packaging designs as they better support power-integrity challenges brought on by advanced computing and memory-bandwidth demands. The techniques leverage the presence of parasitic inductance present in the package or/and MLCC, rather than employ external inductances.

REFERENCES

[1] Le, Hanh-Phuc, Seth R. Sanders, and Elad Alon. “Design techniques for fully integrated switched-capacitor DC-DC converters.” *IEEE Journal of Solid-State Circuits* 46, no. 9 (2011): 2120-2131.

[2] Sanders, Seth R., Elad Alon, Hanh-Phuc Le, Michael D. Seeman, Mervin John, and Vincent W. Ng. “The road to fully integrated DC-DC conversion via the switched-capacitor approach.” *IEEE Transactions on Power Electronics* 28, no. 9 (2012): 4146-4155.

[3] Cervera, Alon, Michael Evzelman, Mor Mordechai Peretz, and Shmuel Ben-Yaakov. “A high-efficiency resonant switched capacitor converter with continuous conversion ratio.” *IEEE Transactions on Power Electronics* 30, no. 3 (2014): 1373-1382.