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POWER SAVING ARCHITECTURE FOR WIRELESS CHARGER

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Power Saving Architecture for Wireless Charger

ABSTRACT

Wireless Charging become popular overtime to the mobile products, All in One (AIO) PC usually embedded Wireless Charger inside the stand and Wireless Charger is required to standby at S4/S5 PC OFF Mode.

Standby power consumption of Wireless Charger is high (around 150mW) which cause PC not able to meet ERP-LOT3 S5 regulatory requirement. (S5 Power < 1W)

Exist strategy on AIO PC is simply disable Wireless Charger at S4/S5 which negatively impact user experience, the invention is to propose a new power architecture helping AIO PC enable wireless charger at S4/S5 without risk failing ERP-LOT3 S5 regulatory.

DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a typical block diagram for the invention.

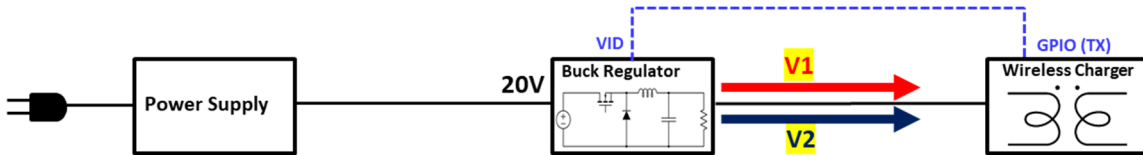


Table. 1 illustrates the wireless charger control mode.

VID	Buck Regulator Output	MODE
H	V2	CHARGE MODE
L	V1	STANDBY MODE

The Ideal Concept of Power Saving Architecture requires

- A Buck Regulator support dynamic Output Voltage Changes
- Wireless Charger GPIO control Buck Regulator VID depends on Standby Mode or Charging Mode.

STANDBY MODE (V1)

At Standby Mode, VID = L, Buck Regulator output V1, Wireless Charger takes V1 to detect if any phone attached, V1 typically will be low voltage. (3.3V, 5V..etc).

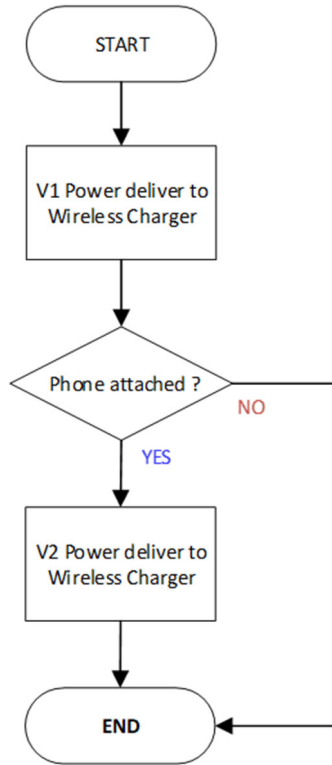
Optimal V1 value can be determined by Buck Regulator and Wireless Charger overall power loss.

CHARGE MODE (V2)

At Charging Mode, VID = H, Buck Regulator output V2, Wireless Charger takes V2 to charge phone attached, V2 typically will be high voltage. (10V, 12V..etc).

Optimal V2 value can be determined by Buck Regulator and Wireless Charger overall power loss.

Fig. 2 illustrates a flow chart of the invention proposal.



Disclosed by Angus Liu, Steve Chen and Jerome Bove, HP Inc.