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SAWTOOTH GENERATOR CIRCUIT TO APPLY SLOPE-COMPENSATION ON CONTROL SIGNAL FOR DC-DC CONVERTER UNDER DIGITAL PCMC SCHEME

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Sawtooth generator circuit to apply slope-compensation on control signal for DC-DC Converter under Digital PCMC Scheme

Abstract

DC-DC converters are needed to efficiently convert between different voltage levels within the electrical architecture of LFP (Large Format Printing) products. Traditionally, analog solutions have been presented to implement the controller of the converter, but this solution presents several limitations in terms of flexibility, modularity, etc.

To overcome these limitations, digital solutions, for instance based in a MCU (microcontroller) are being proposed, since new applications in the field of power electronics can be targeted with MCUs at a very competitive cost, due to the advances of these devices not only in terms of computational and memory features, but also in terms of embedded peripherals such as comparators, DACs, operational amplifiers, etc.

When a DC-DC Boost Converter is controlled with a PCMC (Peak Current Mode Control) scheme, subharmonic oscillations can occur. To overcome this issue, slope-compensation must be implemented, which consists of adding an additional slope to the sensed inductor current signal. When the inductor current is sensed on the HS (High-Side), it is preferred to implement the slope compensation by subtracting this additional slope to the control signal. In more advanced MCUs, sawtooth generators are usually embedded in the DAC channels employed for the control signal generation, so that slope-compensation can be easily implemented. However, these MCUs are usually out of scope when low-cost is targeted.

In consequence, this works presents a simple electronic solution to implement slope-compensation by subtracting a sawtooth signal from the control signal, mainly based in a capacitor and a discharge current source. Three possible implementations are presented for the current source, trading-off complexity, and performance.

1. Introduction

DC-DC converters are needed within Large Format Printing environments to efficiently convert between different voltage levels within the electrical architecture of these products. One example are architectures where the printer is DC supplied via a 12V PSU (Power Supply Unit), and higher voltages are needed to drive printer mechatronics (for instance 24 V, 32 V and 42 V). In this case, one or various DC-DC Boost Converters are needed to step-up the voltage, as depicted on Figure 1.

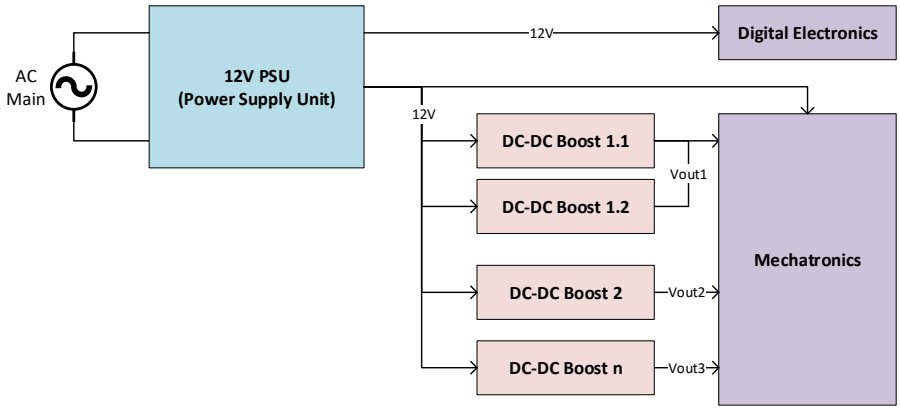

Figure 1. Typical simplified power architecture of Large Format Printing products targetting low cost.

Since this architecture is commonly stated for different products targetting low-cost, DC-DC Boost Converters should be designed in a modular way, so that they can be employed in applications with different requirements in terms of power: different output voltages, power capabilities, etc. Ideally, fully reusable modules are desired, so that with any hardware changes the modules can be instantiated on different electrical designs targetting different power specifications.

Common solutions presented up to now consists of analog controller ICs (Integrated Circuits), which are commercial chips that completely or partially embed all the circuitry needed for the control of the DC-DC Converter. Particularly, LM5122 IC – based solution, which implements a PCMC (Peak Current Mode Control) for DC-DC Boost Converter has been employed within different products. However, this solution presents the following main limitations:

- Although the analog controller can be tuned by means of external components, it offers a limited design flexibility (it depends on the internal topology of the commercial IC).
- Its modularity is limited, since although a design with the same layout and therefore PCB (Printed Circuit Board) can be stated for DC-DC Converter modules targetting different output voltages, a different BoM (Bill of Material) is needed for each case and therefore a different PCA (Printed Circuity Assembly), thus reducing overall production volumes (and therefore increasing overall production costs). Additionally, each PCA must be independently certified, which increases development costs, risks, and times.
- Implementation of protections, diagnostics and other advanced-control features may require of additional circuitry, thus increasing solution complexity and cost.
- It exists a high dependence on the analog Controller IC, which can lead to EoS (End of Support) or EoL (End of Life) issues.

To overcome these limitations, implementing the controller in the digital domain for instance in a MCU (Microcontroller) is an interesting solution, so that:

- Controller can be completely tuned by means of embedded firmware/software.
- The design can be fully modular if conveniently designed, so that different specifications can be covered by means of conveniently adjusting firmware/software with the same hardware, and therefore having a single PCA that can be reused for different power requirements.

- Implementation of protections, diagnostics and other advanced-control features can be implemented in the same MCU.
- Risk associated to EoL and EoS issues is minimized since there are different MCUs which can be easily compatibilized.

Nowadays MCUs embed different peripherals which can be used for control implementation (comparators, ADCs, DACs, Timers, etc.). However, it usually exists a trade-off between cost and peripheral availability.

Due to this fact, a common approach to control a DC-DC Boost Converter is to implement a Digital PCMC scheme where the outer-loop voltage compensator (which sets the output voltage, converter dynamics, etc.) is implemented in the digital domain (by means of embedded software in the MCU) and the inner inductor peak current control loop is implemented in the analog domain, with embedded and/or external circuitry. In this aspect, two options are usually stated: HS (High-Side) current sensing and LS (Low-Side) current sensing. These two approaches are depicted on Figure 2 and Figure 3 respectively.

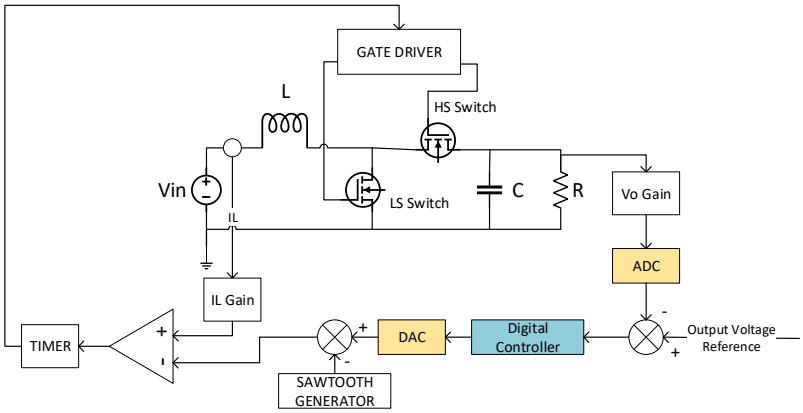

Figure 2. DC-DC Boost Converter under Digital PCMC when current sense is implemented on the HS, and slope compensation is applied on the control signal that sets the targeted peak inductor current.

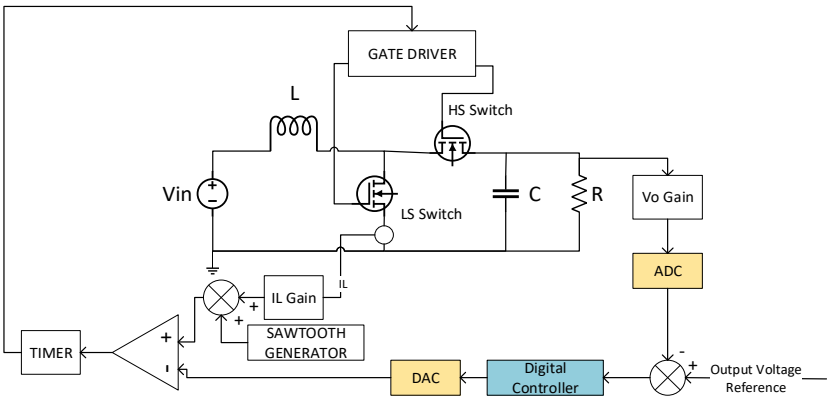

Figure 3. DCDC Boost Converter under Digital PCMC when current sense is implemented on the LS, and slope compensation is applied directly on the sensed inductor current.

For a DC-DC Boost Converter, the HS current sense approach is usually preferred, since transients in the sensed inductor current due to LS switch switching events are minimized by sensing a continuous current.

When a DC-DC Boost Converter is controlled with a PCMC scheme, subharmonic oscillations can occur when the duty cycle of the control signal driving the LS switch is lower than 50%, which leads to inadequate operation due to instability issues. To avoid that, slope-compensation is required, so that an additional slope must be added to the sensed inductor current signal. This can be done by directly adding it to the sensed inductor signal or by

subtracting it to the control signal, being this second option the preferred option in the HS current sense approach.

To implement the slope compensation by subtracting a certain amount of slope on the control signal a sawtooth generator is needed. The generated sawtooth signal (which must be synchronous with the PWM signals driving the DC-DC Converter switches) is subtracted from the control signal as depicted on Figure 2.

In more advanced MCUs, sawtooth generators are usually embedded in the DAC channels employed for the control signal generation so that slope-compensation can be easily implemented. However, employing these MCUs is usually an overkill for solutions targetting low-cost. Therefore, solution cost can be reduced by employing simpler MCUs and implementing the slope-compensation circuitry externally.

In consequence, this article presents a simple electronic solution implemented by means of basic external components to implement slope-compensation on PCMC HS inductor current sense approach by subtracting a sawtooth signal from the control signal. This solution, which is based on a HS switch implemented via a PNP-BJT switch, a capacitor, and an adjustable current source implements an adjustable slope-compensation, which implements a certain amount of slope-compensation over an input control signal according to a second input slope control signal. Within this solution, three sub-solutions are presented, which present a complexity-performance trade-off. The difference between the three solutions consists of how the current source is implemented, as it will be detailly described in further sections.

2. Description

The solution proposed in this article is intended for the digital PCMC scheme provided in Figure 2. Particularly, it presents and implementation for the blocks marked as “Sawtooth Generator” and the adder that subtracts the output of the “Sawtooth Generator” block from the output of the “DAC” which converts to the analog domain the digital output of the “Digital Controller”. The location of the block implemented by the stated solution in this article is marked in red in Figure 4.

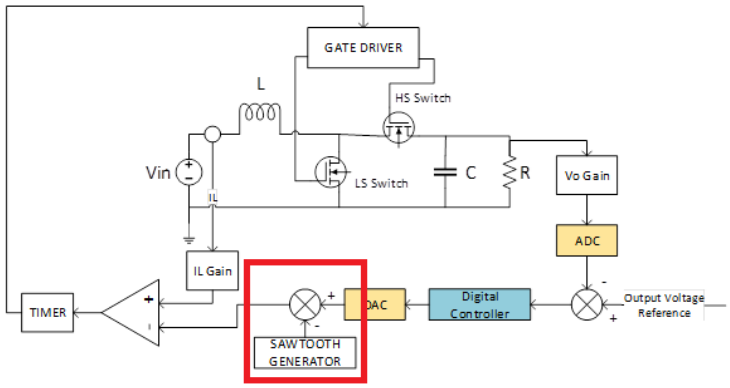

Figure 4. Block implemented by the proposed solution in the digital PCMC scheme.

The general input and output diagram of the proposed solution is presented in Figure 5. In this aspect, the circuit has three inputs:

- $V_{control}$, which stands for the control signal (output of the Digital Controller after D/A (Digital to Analog) conversion).
- V_{slope}, which stands for the signal employed to adjust the amount of slope-compensation to be applied.
- $V_{trigger}$, which stands for the signal that synchronizes the circuit, so that, switching at converter switching frequency f_s, it sets $V_{control,slope}$ to $V_{control}$ when is set to digital ‘0’ value.

The circuit has one single output $V_{control,slope}$ which corresponds to the slope-compensated control signal. The ideal $V_{control,slope}$ is a sawtooth signal with a frequency equal to the switching frequency f_s. The signal reset value (at $t = 0, T_s, 2T_s, \dots$) should be equal to $V_{control}$. The slope of the sawtooth signal is decreasing. The amplitude of the signal is $V_{e,pp}$ and it depends on V_{slope}, so that $V_{e,pp} = g(V_{slope})$, and therefore the amount of slope compensation can be tuned. This behaviour, jointly with the synchronization with $V_{trigger}$ signal is depicted on Figure 6.

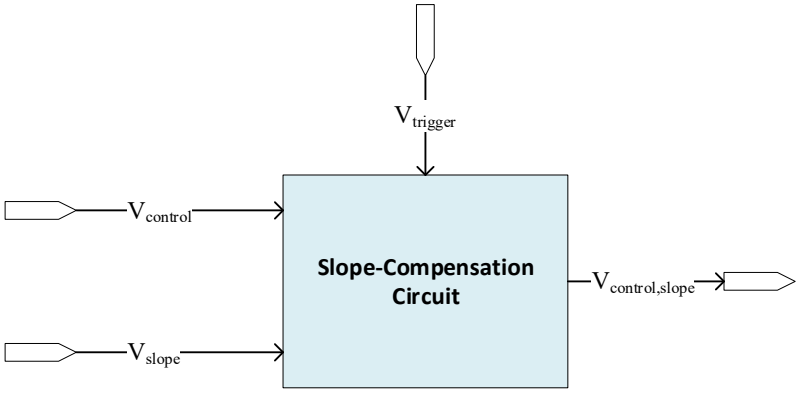

Figure 5. Slope compensation circuit input and outputs.

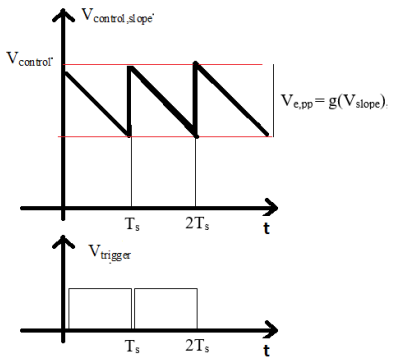

Figure 6. Ideal $V_{control,slope}$ slope-compensated control signal.

The generic implementation of the circuit is depicted on Figure 7. In this aspect, the circuit consists of:

- A buffer, which can be implemented, for instance, by means of an Operational-Amplifier in Source Follower configuration, which can be embedded or not within the MCU DAC.
- A capacitor C1. The voltage at this capacitor is the slope-compensated control signal.
- A PNP BJT Q1, which is controlled via $V_{trigger}$ signal. When $V_{trigger}$ is set to '0', the capacitor is charged via Q1 up to $V_{control}$. The charging process is controlled by means of the polarization set by bias base resistor R1.
- When $V_{trigger}$ is set to '1', the capacitor is discharged by means of the current source $I_{disch.}$ I_{disch} depends on V_{slope}, so that slope-compensation can be tuned by means of the voltage signal V_{slope}.

The amount of slope-compensation S_e can be expressed by (1):

$$S_e = \frac{I_{disch}}{C_1} \tag{1}$$

Therefore, since C_1 is fixed, the amount of slope-compensation can be tuned by means of the discharge current $I_{disch.}$

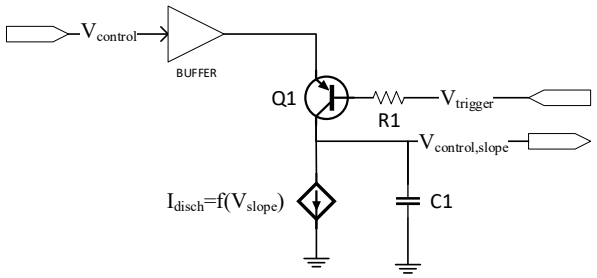

Figure 7. Generic implementation of the proposed slope-compensation circuit.

Three different approaches are presented, which depend on how the current source is implemented, thus presenting a cost-performance trade-off.

2.1. Resistive Discharge

The first approach is implementing the current source by a simple resistor. This solution is depicted on Figure 8. In this aspect:

- It is the simpler solution.
- It presents a trade-off between the achieved linearity, the minimum control voltage $V_{control,MIN}$ and slope-compensation tuning range.

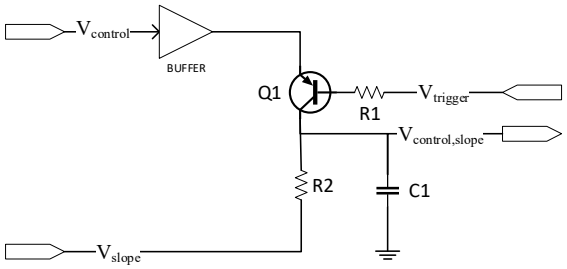

Figure 8. Implementation of the proposed slope-compensation circuit (Approach 1 – Resistive Discharge).

Note that, while the capacitor is being discharged, the slope-compensated control signal can be expressed by means of (2):

$$V_{control,slope}(t) = V_{control} - \left(V_{control} - V_{slope}\right)e^{-\frac{t}{R_2C_1}} \tag{2}$$

Under this approach, the discharge current can be expressed as in (3):

$$I_{disch}(t) = C_1\frac{dV_{control,slope}(t)}{dt} = \frac{V_{control} - V_{slope}}{R_2}e^{-\frac{t}{R_2C_1}} \tag{3}$$

We can define ΔV_c and τ as (4)(5):

$$\Delta V_c \triangleq V_{control} - V_{slope} \tag{4}$$

$$\tau \triangleq R_2C_1 \tag{5}$$

It is worth noting that since the discharge process is exponential, the voltage in the capacitor can be linearly approximated (constant current source) if $\tau \gg T_s$. Under this assumption, the amount of slope compensation S_e can be approximated by (6):

$$I_{disch}(t) \approx I_{disch}(t)_{\tau \gg t} = I_{disch} = \frac{\Delta V_c}{R_2} \rightarrow S_e \approx \frac{\Delta V_c}{\tau} \tag{6}$$

Then, the relative linearity error ϵ can be computed by means of (7):

$$\epsilon = \frac{I_{disch} - I_{disch}(t)}{I_{disch}} = 1 - e^{-\frac{t}{\tau}} \tag{7}$$

Regarding the tuning range for S_e, note for a given range of ΔV_c, which will be determined by the DAC dynamic range, it can be increased by reducing τ. However, reducing τ leads to a worst linearity. Thus, it exists a trade-off between the S_e adjustment range and the achieved linearity.

Additionally, note $\Delta V_c \geq 0 \rightarrow V_{slope} \leq V_{control}$. In a common unipolar supply scheme, $V_{slope} \geq 0$. Thus, a minimum value for $V_{control} \geq V_{control,min}$ should be stated, so that tuning range ΔV_c is available for that worst-case $V_{control,min}$. Therefore, it also exists a trade-off between the minimum voltage allowed on the control signal and the tunability range of the slope compensation S_e.

2.2. NPN BJT Current Source

The second approach consists of implementing the discharge current source by a NPN BJT. This solution is depicted on Figure 9. The most important aspects regarding this implementation are summarized below:

- Linearity is improved by implementing the current source with a basic emitter-degenerated NPN BJT transistor, so that in a first-order approximation discharge current can be considered constant.
- Dependence of the allowable tunability range for S_e on minimum voltage allowed on $V_{control}$ is removed.
- The amount of slope-compensation dependence on NPN BJT transistor current gain β is minimized by employing resistive degeneration.
- The amount of slope-compensation strongly depends on transistor base-emitter turn-on voltage $V_{BE,ON}$, which is expected to typically have a huge systematic and random variability.

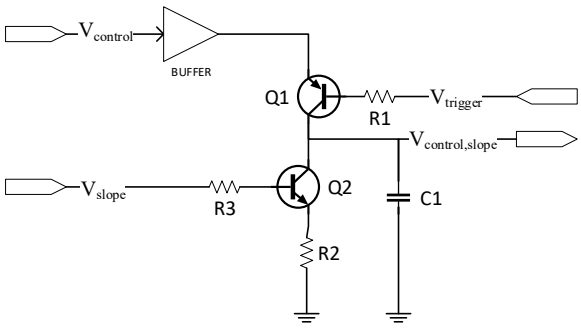

Figure 9. Implementation of the proposed slope-compensation circuit (Approach 2 – NPN BJT Current Source).

In this case, note the discharge current can be assumed to be constant, so that a fully linear response is ideally expected. In practice, due to second-order effects, non-linearities will be observed. The discharge current can be approximated as in (8) by analysing the Base-Emitter junction of NPN BJT transistor:

$$I_{disch} = \beta \frac{V_{slope} - V_{BE,ON}}{R_2(\beta + 1) + R_3} \tag{8}$$

If the BJT gin β is large enough, then it can be approximated to (9):

$$I_{disch} \approx \lim_{\beta \to \infty} I_{disch} = \frac{V_{slope} - V_{BE,ON}}{R_2} \tag{9}$$

And therefore, the amount of slope compensation can be expressed by (10):

$$S_e \approx \frac{V_{slope} - V_{BE,ON}}{R_2 C_1} \tag{10}$$

Therefore, the amount of slope compensation can be tuned by means of V_{slope} without depending on $V_{control}$. If β is large enough (which is usually accomplished), S_e does not depend on it. However, S_e depends on transistor base emitter turn-on voltage, which has strong systematic and random variabilities (thermal dependence, tolerance, etc.).

2.3. NPN BJT Current Source in Negative Feedback Configuration

The lastly proposed approach is an improved solution of the second approach, where the current source implemented by means of an NPN BJT is introduced in a negative feedback loop implemented with an operational amplifier. With that, dependence of S_e on $V_{BE,ON}$ is removed. This circuit solution is depicted on Figure 10.

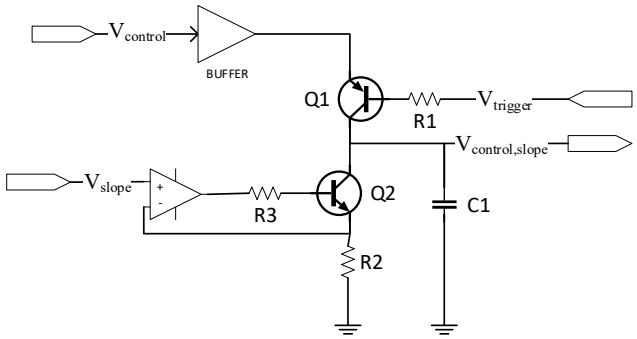

Figure 10. Implementation of the proposed slope-compensation circuit (Approach 3 – NPN BJT Current Source in Negative Feedback Configuration).

The discharge current, in this case, can be estimated by (11) (assuming an ideal Operational Amplifier):

$$I_{disch} = \frac{V_{slope}}{R_2} \tag{11}$$

And the amount of slope compensation (12):

$$S_e = \frac{V_{slope}}{R_2 C_1} \tag{12}$$

Note it does not depend on transistor parameters, which is the main benefit in front of the previously described approach.

3. Advantages of the proposed solution

By employing the solution described in this work, the following advantages can be pointed out:

- The proposed approaches to implement slope-compensation enables the possibility of controlling the DC-DC Boost Converter via digital PCMC scheme implemented in an MCU, which present advantages in front of the analog approach:
  - Controller can be completely tuned by means of embedded firmware/software.
  - The design can be fully modular if conveniently designed, so that different specifications can be covered by means of conveniently adjusting firmware/software with the same hardware.
  - Implementation of protections, diagnostics and other advanced-control features can be implemented in the same MCU so that a standard communication interface can be offered to access to the DC-DC Converter functionalities.
  - Risk associated to EoL and EoS issues is minimized since there are different MCUs which can be easily compatibilized.
- The proposed approach to implement slope-compensation does not require an MCU with advanced DAC capabilities (sawtooth wave generation), which simplifies the requirements of the MCU and potentially the cost of the solution.

- The proposed approach enables PCMC control via HS current sense versus LS current sense, which is preferred in the DC-DC Boost Converter topology due to peak transients produced by low-side switch.
- The proposed approach offers a control signal to tune the amount of slope-compensation to be applied on the control signal so that the design is fully modular, since the amount of slope-compensation can be tuned by means of software via an additional control signal V_{slope}, which can be driven by an additional DAC Channel embedded on the same MCU.

Therefore, it can be concluded that by employing this solution a competitive advantage can be achieved, being aware of the limitations of the described circuitry, which have been detailly pointed out, and several solutions have been proposed within the complexity-performance design space.

Disclosed by Miguel Ángel Alegre López, HP Inc.