October 2020

Voltage Droop Mitigation Using Integrated High Density Capacitor Modules

N/A

Voltage Droop Mitigation Using Integrated High Density Capacitor Modules

ABSTRACT

This disclosure describes techniques for the mitigation of voltage droop in computer processor systems. Per techniques of this disclosure, high-density capacitor (cap) modules with plated through holes (PTH) are integrated into an electronic package and/or a printed circuit board (PCB). The pitch and sizing of the PTH and pads are designed to match external connections. Power to devices is delivered vertically through the capacitance module(s) via the PTHs, without any lateral power distribution, thereby reducing voltage droops within the PDN. The capacitor module is placed directly underneath the point of electrical load, with the PTHs aligned with external connections. Electrical connections are provided at the top and bottom sides of the capacitor module. The capacitor module(s) can be integrated into any thick-core organic substrate packaging and/or a PCB that is more than a few layers thick to significantly increase an equivalent capacitance.

KEYWORDS

- Power delivery network (PDN)
- Voltage droop
- High density capacitor
- Plated through-hole (PTH)
- Ball grid array (BGA)

BACKGROUND

Power delivery networks (PDN) are commonly utilized to provide electrical power to components (devices) in an integrated circuit (IC) module, e.g., computer processor modules, application-specific integrated circuits (ASICs), other IC packages, etc. The power integrity of a

PDN is affected by electrical properties, e.g., capacitance, inductance, resistance of constituent components that are included in the circuit. The PDN commonly includes a power supply (e.g., one or more voltage regulators), which provides power through the printed circuit board (PCB), electronic package and an on-die power grid to the active components (devices).

Resistive or inductive impedances in the PDN can cause transient current spikes that lead to supply voltage droops. These droops can affect device performance since logic delays increase with lower supply voltage, which necessitates greater timing margins in logic and memory cells. In processors designed for computationally intensive operations, e.g., graphics processing units (GPU), machine learning processors, etc., it has been observed that electrical power noise in the circuit is typically determined by components effective at the frequency range of 1-10MHz, which forms a second droop in a step response of the PDN. The resulting second droop limits the minimum nominal voltage setpoint of the power supply and can lead to increased power consumption and negatively affect processor performance.

The second droop is sometimes addressed by increasing capacitance in ASIC packaging and/or decreasing inductance between decoupling capacitors placed in the package and decoupling capacitors located on the PCB. However, the above mentioned techniques face challenges in modern applications. The high power demand of contemporary devices necessitates thicker PCBs which increases the package-to-PCB inductance. Additionally, the amount of capacitance that can be added as die-side-capacitor (DSC) or land-side-capacitor (LSC) is limited by the physical area available on the top and bottom of the package. Addition of LSCs to the bottom of package substrate also requires depopulation of solder balls/pins and creates crowding concerns, e.g., electromigration (EM) damage of the solder ball joints.

DESCRIPTION

This disclosure describes techniques for the mitigation of voltage droop in computer processor systems. Per techniques of this disclosure, high-density capacitor (cap) modules with plated through holes (PTH) are integrated into an application-specific integrated circuit (ASIC) packaging or a PCB to achieve superior electrical performance.

The high-density capacitor modules include plated through holes (PTH) that connect top and bottom pads. The pitch and sizing of the PTH and pads are carefully designed to match external connections. For example, the pitch and sizing of the PTH and pads are selected such that they match the ball grid array (BGA) solder ball pitch and size of the ASIC packaging. Power is delivered to devices vertically through the capacitance module(s) via the PTHs, without any lateral power distribution, thereby reducing voltage droops within the PDN.

The capacitor module can be placed directly underneath the point of electrical load, with the PTHs well aligned with external connections. Electrical connections are provided at the top and bottom sides of the capacitor module.

In designs where the high density capacitor module is integrated into a package substrate, one or multiple cavities or through holes are created in the core layers of the package substrate such that the thickness of the cavity or through hole matches the thickness of the capacitor module. The capacitor module is placed into the cavity or through hole. Additional connections, e.g., micro via-connections, are provided to the top and/or bottom pads if the top and/or bottom interfaces of the capacitor module faces build up layers of the package.

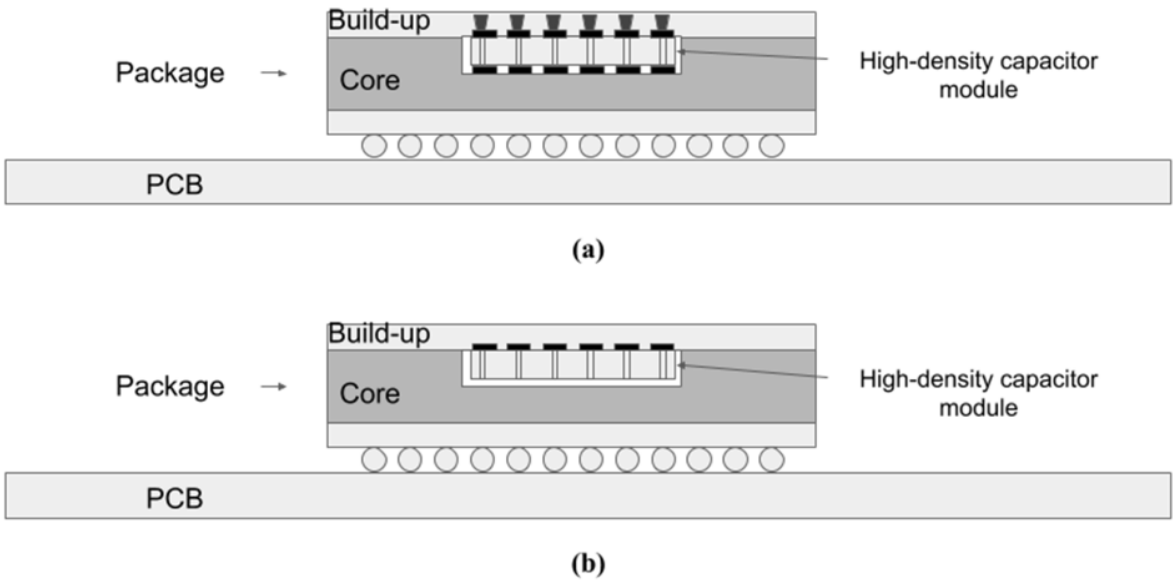

Fig. 1: Cap module integrated into a package core cavity; (a) with pads; (b) without pads

Fig. 1 depicts example configurations of an electronic package and PCB with an integrated high-density capacitor module, per techniques of this disclosure. Fig. 1(a) depicts an example configuration where the high-density capacitor module is integrated into a cavity provided within the package core layer. Pads are provided in the core cavity for dual side electrical connectivity and to enable vertical power distribution through the capacitor module. Fig. 1(b) depicts an example configuration where the high-density capacitor module is integrated into a cavity provided within the package core layer, without any additional pads. In this configuration, direct current (DC) is not routed via the high density capacitor module.

As depicted in Fig. 1(b), if the bottom interface of the module faces the inner core layer (e.g., when the capacitor module is integrated into a cavity in the package core), either the bottom pads of the module are not connected, or a layer of pads is added on the bottom of the cavity, and an electrical connection is made between the pads of the capacitor module and the cavity.

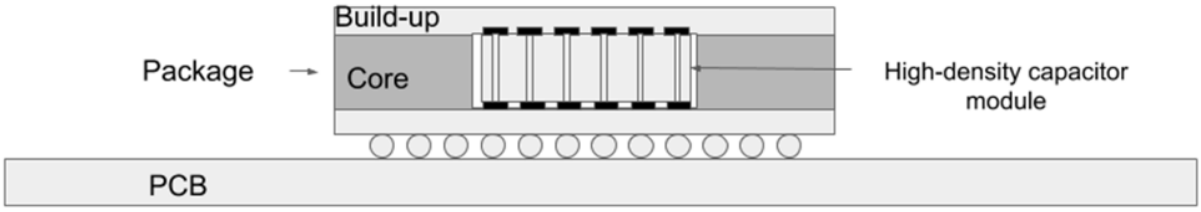

Fig. 2: Cap module integrated into a package core using a through hole

Fig. 2 depicts an example configuration where a capacitor module is integrated into a through hole provided in the package core. The through hole enables utilization of larger capacitances that can provide superior electrical performance.

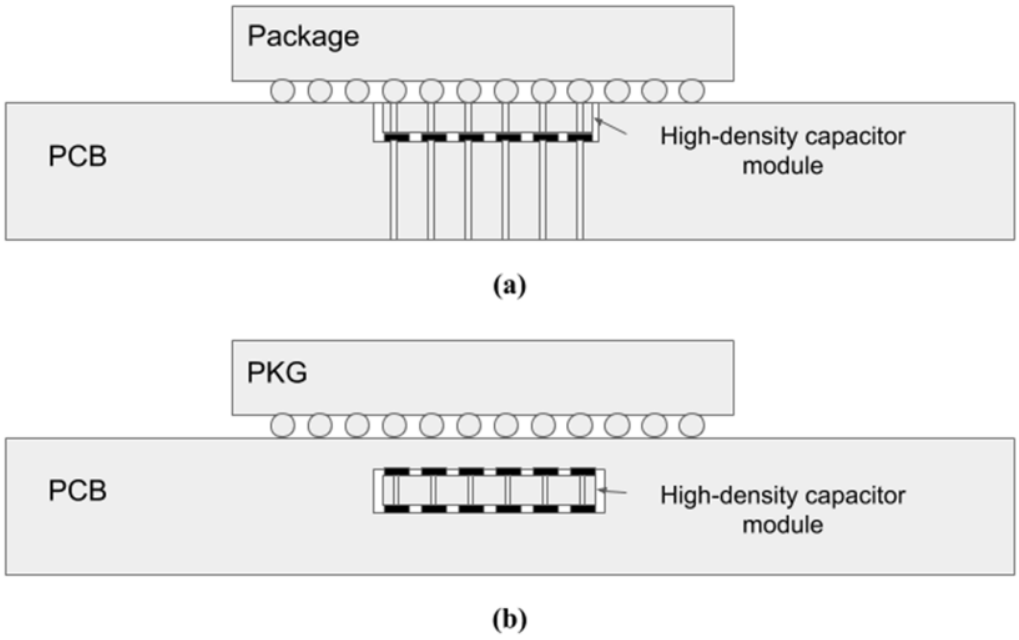

Fig. 3: Integration into a PCB surface cavity; (a) top layer; (b) inner layer

Fig. 3 depicts example configurations where the high-density capacitor module is integrated into a PCB surface. Fig. 3(a) depicts an example configuration where the capacitor module is integrated into a top layer of the PCB surface. Fig. 3(b) depicts an example configuration where the capacitor module is integrated into an inner layer of the PCB surface.

One or more surface or embedded cavities are created at the top, bottom, or in the inner layers of the PCB, with dimensions matched to the capacitor module. The capacitor module is placed into the cavity. If the top or bottom interface of the cap module faces internal layers of the PCB, a layer of pads is added in the PCB cavity, making electrical connections (e.g., through solder) to the cap module pads. If the top or bottom interface of the module faces an external component, such as a ball grid array (BGA) interface of a chip or power module, the solder joints are formed directly between the external component and the pads of the cap module.

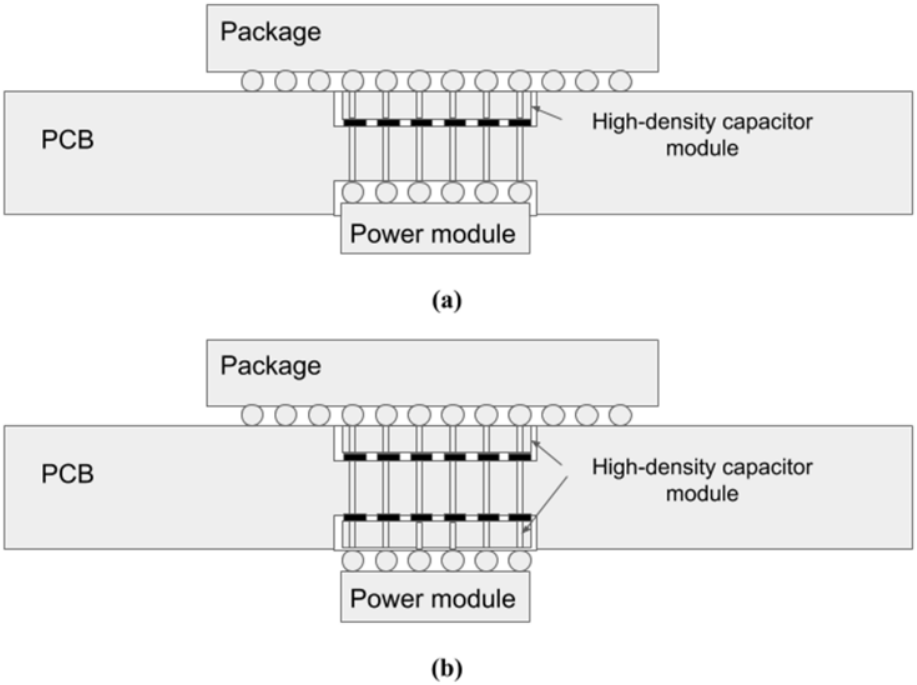

Fig. 4: Cap module integration with vertical power delivery

Fig. 4 depicts example configurations where the high-density capacitor module is integrated into a PCB surface along with vertical power delivery (VPD). Vertical power delivery can reduce PDN resistance and enable better processor performance in high processor current conditions. As depicted in Fig. 4(a), the capacitor module is placed in a cavity in the PCB surface. A vertical power module is placed directly beneath the capacitor module at an opposite

side of the PCB. An optional cavity can be provided in the PCB surface to place the vertical power module. Fig. 4(b) depicts an example configuration that includes two high density capacitor modules.

Integration of the capacitor module at a location proximate to a vertical power module enables potential elimination of a separate capacitor layer that is usually deployed in vertical power module design. This results in thinner vertical power modules, easier manufacturing and assembly since no multi-layer structure is needed, and potentially better thermal/mechanical performance.

The techniques of this disclosure are particularly suitable when a mid-frequency second droop is a limiting factor in power integrity design. The capacitor module(s) can be integrated into any thick-core organic substrate packaging and/or a PCB that is more than a few layers thick to significantly increase an equivalent package capacitance. For example, in some advanced processors, the capacitance value can be increased by more than 400% with integration of a moderately sized capacitor module integrated into the package. The second droop issue can be completely eliminated in some systems.

Additionally, no BGA depopulation is needed to create space to house the capacitor modules, since the modules are placed into cavities in the substrate or PCB. Thus, there is minimal impact to the inductance and resistance along the PDN, and no local current crowding effect is expected since the DC current path is not interfered, unlike in traditional techniques, e.g. use of land side capacitors (LSC).

CONCLUSION

This disclosure describes techniques for the mitigation of voltage droop in computer processor systems. Per techniques of this disclosure, high-density capacitor (cap) modules with

plated through holes (PTH) are integrated into an electronic package and/or a printed circuit board (PCB). The pitch and sizing of the PTH and pads are designed to match external connections. Power to devices is delivered vertically through the capacitance module(s) via the PTHs, without any lateral power distribution, thereby reducing voltage droops within the PDN. The capacitor module is placed directly underneath the point of electrical load, with the PTHs aligned with external connections. Electrical connections are provided at the top and bottom sides of the capacitor module. The capacitor module(s) can be integrated into any thick-core organic substrate packaging and/or a PCB that is more than a few layers thick to significantly increase an equivalent capacitance.