Hybrid Lidded Multi-Chip Package
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ABSTRACT

This disclosure describes a hybrid lidded multi-chip package that includes a non-continuous lid that is matched to corresponding thermal requirements of different chips in the package. Per techniques of this disclosure, selected portions of the chip package where cooling requirements can be met when lidded include a lid, whereas portions of the chip package that require additional cooling that may be hampered by a lid do not include a lid. Portions requiring additional cooling utilize the opening in the lid design that enables the chip to be directly in contact with a heat sink (cold plate) and a second thermal interface material. Suitable modifications are provided in the cold plate pedestal design to accommodate variable depths in the chip package. Different thermal interface materials that are tailored to the thermal requirements at different chip locations are utilized. Described configurations can provide a combination of superior thermal performance and reliability.

KEYWORDS

- Lidded package
- Multi chip package
- Thermal management
- Thermal resistance
- Thermal interface material (TIM)
- Warpage
- High bandwidth memory (HBM)
- Hybrid cold plate
BACKGROUND

Modern computing devices commonly include multi-chip (integrated circuit) packages for their processing requirements in which multiple chips are integrated using a common substrate and which function as a single integrated circuit. Thermal expansion differences between the chips and the substrate can lead to package warpage. This is usually mitigated by the use of lidded packages, where a copper or other lid is mounted to the chip (die) for added structural strength. A thermal interface material (TIM) is provided between the lid and the chip to eliminate interstitial air gaps at the interface and to improve heat transfer away from the chip.

Fig. 1: Schematic of lidded chip package

Fig. 1 illustrates an example lidded chip package that depicts two chips mounted onto a substrate. A lid is mounted to the chip with a thermal interface material layer provided to improve heat dissipation. A cold plate is attached to the lid to absorb heat away from the package.

However, certain high performance chips such as chips utilized in high computational performance applications (e.g., machine learning) dissipate high power and require advanced cooling techniques to maintain performance and reliability. There can also be a buildup of heat...
flux due non-uniform power distribution within the package. One approach for advanced cooling is to reduce thermal resistances between the die (silicon) and heat sinks by removing the lid on the package. However, removal of the lid can lead to increased warpage and adds to reliability concerns since the high performance chips typically also have a larger package size.

**DESCRIPTION**

This disclosure describes a hybrid lidded multi-chip package that includes a non-continuous lid that is matched to corresponding thermal requirements of different chips in the package. Per techniques of this disclosure, customized openings in the lidded package are provided at chip locations with high heat dissipation, while other portions of the chip package that generate less heat are lidded. The openings in the lid design enable portions that require additional cooling to be directly in contact with a heat sink (cold plate) and a second thermal interface material.

Suitable modifications are provided in the cold plate pedestal design to accommodate variable depths in the chip package along with the use of different thermal interface materials that are tailored to the thermal requirements at different chip locations. Some example configurations for the hybrid lidded multi-chip package are described below.
Fig. 2: (a) Side view of cold plate and chip package; (b) Top view

Fig. 2(a) and 2(b) depict side and top views, respectively of a first example configuration of a hybrid lidded multi-chip package with customized openings, per techniques of this disclosure. As depicted in Fig. 2(a), customized openings are provided for the higher power dissipation chips- chip 1 and chip 3 - which are configured to be in direct contact with a cold plate. A first thermal interface layer (TIM1), for example, of graphite, is provided, e.g. laminated, coated, etc., on all the chips. Chip 2 is attached to a lidded portion of the package, which in turn is configured to be in contact with the cold plate. A second thermal interface layer (TIM2), for example, of a grease based material is utilized to connect the lidded portion of the
package to the cold plate. The cold plate is configured with variable channel depth to ensure a uniform surface at the top of the cold plate. The channel depths of the cold plate are deeper and shallower.

Fig. 2(b) depicts a top view of this configuration. As depicted in Fig. 2(b), chip 2 is obscured by the lidded portion of the package whereas chip 1 and chip 3 are exposed from above since they are located in the non-lidded portion of the package.

![Diagram of a hybrid lidded multi-chip package](image)

**Fig. 3:** (a) Side view of cold plate and chip package in a second configuration; (b) Top view

Fig. 3(a) and 3(b) depict side and top views, respectively of a second example configuration of a hybrid lidded multi-chip package, per techniques of this disclosure. In this
example configuration, a customized opening is provided for the higher power dissipation chip, chip 2, which is configured to be in direct contact with a cold plate. Chip 1 and chip 3 are attached to lidded portions of the package, which in turn is configured to be in contact with the cold plate.

Fig. 3(b) depicts a top view of this configuration. As depicted in Fig. 3(b), only chip 2 is exposed from above since it is located in the non-lidded portion of the package, while chip 1 and chip 3 are obscured by the lidded portion of the package.

![Diagram of chip configuration](https://www.tdcommons.org/dpubs_series/3656)

**Fig. 4: Third configuration with TIM1 use at selected chip locations**

Fig. 4 depicts a third example configuration, per techniques of this disclosure. In this illustrative example, TIM1 is utilized at select chip locations, e.g. on chip 1, when compared to earlier described configurations where TIM1 was utilized on all chips. TIM2 is utilized on the lidded portion and on the exposed chips, in this case, chip 1 and chip 3.
Fig. 5: Example configuration for high bandwidth memory (HBM) chip packages

Fig. 5 depicts an example configuration for use in high bandwidth memory (HBM) chip packages, per techniques of this disclosure. HBM chips have relatively stringent thermal requirements when compared to other chips. Accordingly, the cold plate utilizes a greater base thickness for portions at the contact locations with the HBM chips. As depicted in Fig. 5, the hybrid lid provides customized openings for the HBM chips, which utilize a layer of TIM2 and is in direct contact with the cold plate.
Fig. 6: Example configuration with TIM1 and TIM2 used on all surfaces

Fig. 6 depicts another example configuration of a hybrid lidded multi-chip package, per techniques of this disclosure. In this example configuration, a TIM1 layer is utilized on all chips, while a TIM2 layer is utilized on the lidded portion as well as on any exposed TIM1 layers. In some implementations, a bonding layer may be utilized in lieu of the TIM 2 layer in the non-lidded portions of the package.

The various configurations described in this disclosure provide a combination of superior thermal performance and reliability due selective openings in the lid as well as from the use of novel thermal interface material combinations. Other configurations that utilize the principles described herein are possible.

CONCLUSION

This disclosure describes a hybrid lidded multi-chip package that includes a non-continuous lid that is matched to corresponding thermal requirements of different chips in the package. Per techniques of this disclosure, selected portions of the chip package where cooling
requirements can be met when lidded include a lid, whereas portions of the chip package that require additional cooling that may be hampered by a lid do not include a lid. Portions requiring additional cooling utilize the opening in the lid design that enables the chip to be directly in contact with a heat sink (cold plate) and a second thermal interface material. Suitable modifications are provided in the cold plate pedestal design to accommodate variable depths in the chip package. Different thermal interface materials that are tailored to the thermal requirements at different chip locations are utilized. Described configurations can provide a combination of superior thermal performance and reliability.