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A Five-metal Layered High-Speed Silicon Interposer with Low Insertion Loss and Cross-Coupling

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ABSTRACT

A silicon interposer is a widely used communications channel, or interconnect, between dies of integrated circuits. When used to connect high-speed application-specific integrated circuits (ASICs) and high-bandwidth memories (HBM), the traditional three-metal layered silicon interposer suffers from excessive insertion loss, cross-talk, and inter-symbol interference. Communications at the requisite speed, e.g., 3 Gbps or more, is unfeasible.

This disclosure describes techniques of optimal dimensioning and placement of traces within a five-metal layered silicon interposer to achieve a robust interposer communications channel with low insertion loss, cross-talk, and inter-symbol interference. ASIC-HBM communications speed of up to 3.6 Gbps is supported with use of the described interposer.

KEYWORDS

- Silicon interposer
- Application-specific integrated circuit (ASIC)
- High-bandwidth memory (HBM)
- Signal trace
- Inter-symbol interference
- Cross-coupling
- Cross-talk
- Insertion loss

BACKGROUND

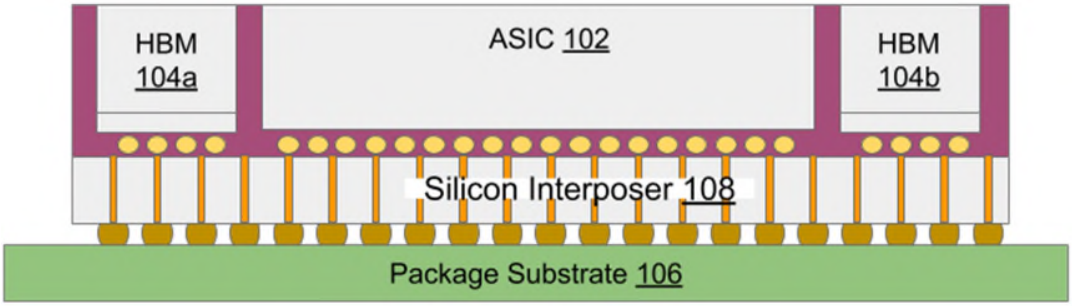

Fig. 1: An interposer used for data communications

Fig. 1 illustrates a typical configuration of an application-specific integrated circuit (ASIC 102) coupled to one or more high-bandwidth memories (HBMs 104a-b) on a package (106). The ASIC and the HBM communicate via a silicon interposer (108) at speeds typically in the range of 1-3 Gbps. A silicon interposer is a widely used communications channel, or interconnect, between dies of integrated circuits.

Recent high-bandwidth memories have a speed of about 3.2-3.6 Gbps, which is about 33-50% faster than that of the previous HBM generation. The increased memory speed is accompanied by a shrinking of the operational timing window by a similar fraction, e.g., 33-50%. To accommodate increased HBM speeds, the interposer channel length is increased, e.g., by approximately 1mm, in its X-dimension, while the total length of the communications channel is increased beyond 5mm. However, silicon interposer traces, especially those less than 2.5 micrometers in width and spacing, are lossy, and compared to conventional substrate channels, subject to interference from cross-coupled channels. Besides, silicon interposers of a dimension appropriate to the most-recent HBM are found to suffer from inter-symbol interference.

DESCRIPTION

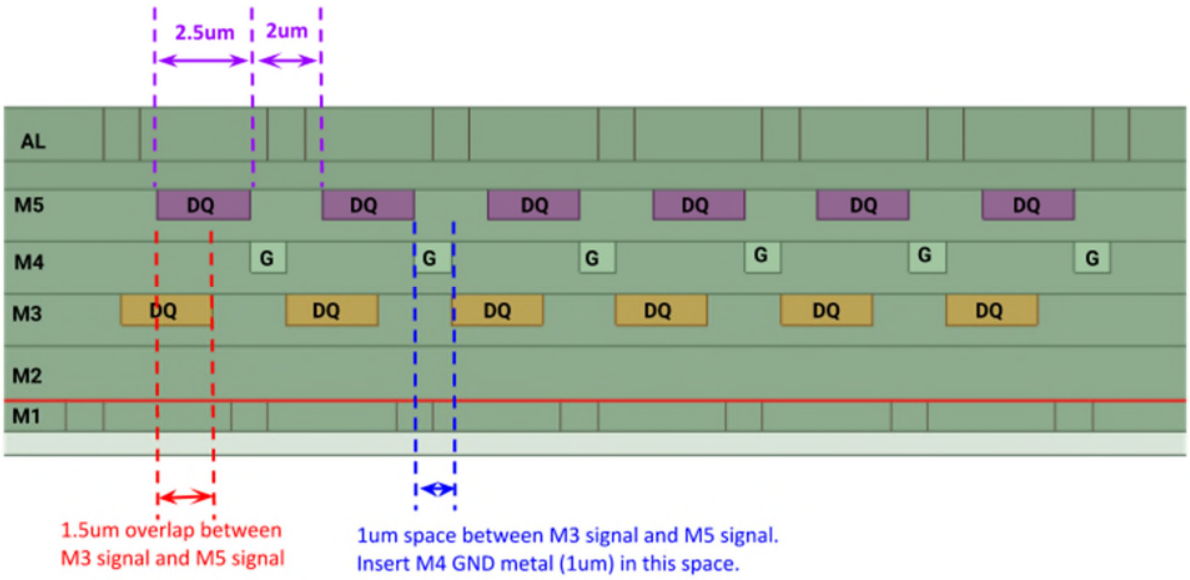

Fig. 2: Cross-section of a five-metal layered, low-loss, low-crosstalk silicon interposer channel that is robust to inter-symbol interference

Fig. 2 illustrates the cross-section of a five-metal layered (5 Mz), low-loss, low-crosstalk silicon interposer channel robust to inter-symbol interference, per the techniques of this disclosure. The metal, e.g., copper, layers are indicated by the symbols M1 through M5. There can be an aluminum pad layer, indicated by AL. Data-line (signal) traces, which carry communications between the ASIC and the HBM are indicated by DQ, and ground traces are indicated by G.

Channel (insertion) loss and inter-symbol interference are reduced by minimizing the channel resistance and capacitance. Channel resistance can be reduced by widening the widths of the signal-carrying traces, e.g., to 2.5 micrometers (μm) as illustrated; however, this also results in an increased capacitance. Capacitance is lowered by avoiding overlaps between signal-carrying traces and the power or ground meshes. For example, as illustrated, a 1 μm spacing

between the M3 and M5 signal-traces enables the positioning of an M4 ground trace of width 1 µm without causing an overlap between the M3 and M5 signal traces.

Cross-talk is reduced by minimizing the coupling between channels and by shielding ground traces. This results in a lower coupling between signals traveling on the various parallel channels, but can result in an increased capacitance. Again, the capacitance is reduced by reducing direct overlap in between signal-carrying traces and between signal-carrying and ground-shield traces. For example, the illustrated design indicates an M3-M5 signal-trace overlap of as little as 1.5 µm and an inter-signal-trace separation between of 2 µm.

The dimensions of the signal traces, the inter-signal-trace distance, etc., are thus optimally balanced to reduce the resistance and the capacitance of the traces. Coupling between traces is substantially reduced by reducing the overlaps in between signal traces and between the signal and ground traces, etc., e.g., by staggering (offsetting) the signal and the ground metal insertion patterns.

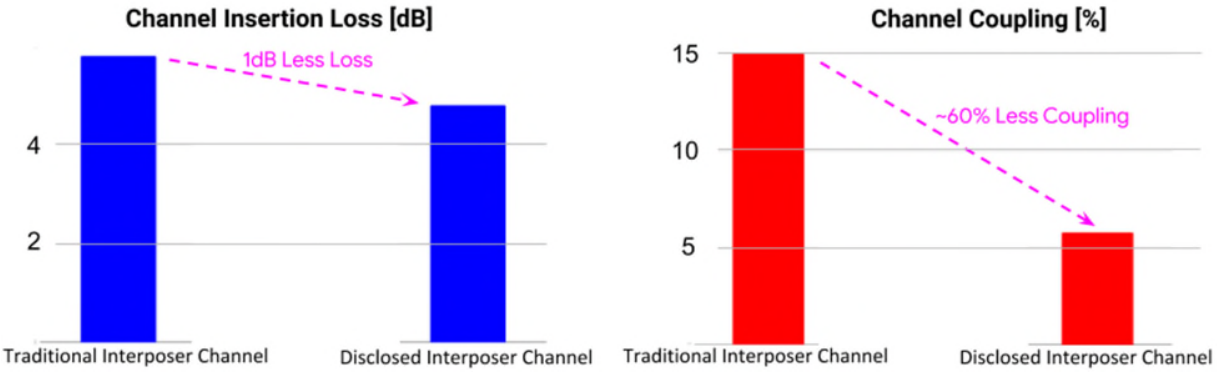

Fig. 3: Illustration of lower loss and channel coupling

As illustrated in Fig. 3, the techniques result in a reduction in channel insertion loss by 1 dB, and a reduction in channel coupling by 60% compared to a traditional interposer.

	Eye-widths at two process corners (pico-secs)	Margin (ps) compared to a TX (at HBM) and RX (at ASIC) of 112 / 64 ps
Traditional interposer without phy offset	158 / 192	158 − (112+64) = −18; 192 − (112+64) = +16
Disclosed interposer without phy offset	210 / 221	210 − (112+64) = +34; 221 − (112+64) = +45
Traditional interposer with phy offset	153 / 167	153 − (112+64) = −23; 167 − (112+64) = −9
Disclosed interposer with phy offset	205 / 212	205 − (112+64) = +29; 212 − (112+64) = +36

Table 1: Illustrating an opened eye pattern with improved timing/voltage margins

Table 1 illustrates an increased opening of the eye pattern of the disclosed interposer, e.g., a lower inter-symbol interference and better timing/voltage margins, compared to traditional interposers. For effective HBM-ASIC communication 3.3-3.6 Gbps, the width of the eye is at least about 112 pico-seconds at the transmit side and at least about 64 pico-seconds at the receive side, e.g., the total eye-width is at least about 112+64 = 176 ps.

For the traditional interposer without phy offset, e.g., a relatively short channel length, the achieved eye-widths at two process corners are 158 ps and 192 ps, such that the margin at one process corner is negative (−18 ps), or non-existent. For the interposer described herein, without phy offset, the achieved eye-width margins at all process corners are healthily positive, e.g., between 34 and 45 ps.

For the traditional interposer with phy offset, e.g., a relatively long channel length, the achieved eye-widths at two process corners are 153 ps and 167 ps, so that the margins at both process corners are negative (−23 and −9 ps), or non-existent. For the interposer described

herein, with phy offset, the achieved eye-width margins at all process corners are healthily positive, e.g., between 29 and 36 ps.

In this manner, by proper dimensioning of the traces within an interposer, and by optimizing the overlaps between traces and ground or power meshes within the interposer, the techniques of this disclosure provide a robust silicon interposer communications channel with low insertion loss, low cross-talk, and low inter-symbol interference.

Alternatively, the interposer may include as signal traces Mi metal, e.g., of approximately 1.5 μm thickness, instead of Mz metal, which is of 0.85 μm thickness. Also, a three-metal layered interposer can be used for lower bandwidths.

CONCLUSION

This disclosure describes techniques of optimal dimensioning and placement of traces within a five-metal layered silicon interposer to achieve a robust interposer communications channel with low insertion loss, cross-talk, and inter-symbol interference.