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INTELLIGENT THUNDERBOLT DOCK LTR SETTING

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Intelligent Thunderbolt Dock LTR Setting

Abstract: Latency Tolerance Reporting (LTR) settings of a dock are changed dynamically in the OS in order to mitigate user interface issues among various devices connected to the dock.

This disclosure relates to the field of computer interfacing.

A technique is disclosed that changes Latency Tolerance Reporting (LTR) settings of a dock dynamically in the OS in order to mitigate user interface issues among various devices.

It is desirable for a Thunderbolt (TBT) dock that expands IO ports to support various components with different bus architectures. The system firmware of a computer that supports a Thunderbolt dock will initiate LTR settings for the Thunderbolt host controller in POST phase in order to make multiple components with different bus interfaces that are connected to the dock work properly together.

However, when a bridge or device connected to the Thunderbolt dock does not support LTR, the user experience will be impacted. The user can experience user interface lag, or meaningless garbage may be displayed on the screen. In addition, a Thunderbolt dock system may still have problems even if all bridges and devices support LTR, due to difficulties in coordinating components that have different LTR settings and slew rates.

According to the present disclosure, LTR settings are dynamically changed in the OS. When a TBT dock is connected to the system, the PD asks the EC to trigger an OS event registered by the BIOS. Then, the BIOS assigns a new LTR setting to the PCIE root port (RP) which services TBT. When the TBT dock is unplugged, the BIOS can restore the LTR value through the same channel.

When the user plugs in the dock to the computer system, the following occurs:

- 1) The PD senses that the TBT dock is plugged in and notifies the EC.
- 2) The EC triggers a Q event registered during pre-boot to the OS.
- 3) The OS executes BIOS code according to the Q event.
- 4) The BIOS saves the current LTR to the BIOS SPI ROM, and sets the new LTR value to the PCIE RP for TBT.

When the user unplugs the dock from the computer system, the following occurs:

- 1) The PD senses that the TBT dock is unplugged and notifies the EC.
- 2) The EC triggers a Q event registered during pre-boot to the OS.
- 3) The OS executes BIOS code according to the Q event.
- 4) The BIOS retrieves the prior LTR value from the BIOS SPI ROM where it was saved, and sets the prior LTR value to the PCIE RP for TBT.

The disclosed technique advantageously enhances the ecosystem of a Thunderbolt docking station. It improves the compatibility among various devices connected to the docking station, and ensures a smooth user experience.

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