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Automated calculation of spacing constraints in multi-layer PCB design

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ABSTRACT

A multi-layer PCB comprises one or more layers made of conducting shapes sandwiched between dielectric layers. The spacing between conducting shapes on a layer is constrained to optimize signal integrity and minimize cross-talk. Such spacing constraints are typically manually calculated and entered into a design tool that enforces the constraints during the design process. Spacing constraints depend on a variety of parameters, including dielectric thicknesses, type of conducting shapes, signal technology, voltage, waveform type, data rate, etc. Manually calculating and maintaining the spacing constraint set across a multi-dimensional matrix of possible values is onerous and error-prone. Engineers frequently simplify the design process by assuming worst-case spacing constraints; the result is a sub-optimally dense PCB. This disclosure describes techniques to automatically calculate spacing constraints given the dielectric thicknesses, conducting shape-pairs, and other parameters. The techniques enable design of efficient, high-density PCBs with excellent signal integrity.

KEYWORDS

- Printed circuit board (PCB)
- Multi-layer PCB
- Computer-aided design (CAD)
- Signal integrity
- Spacing constraint set
- Spacing constraint manager
- Electronic design automation (EDA)

BACKGROUND

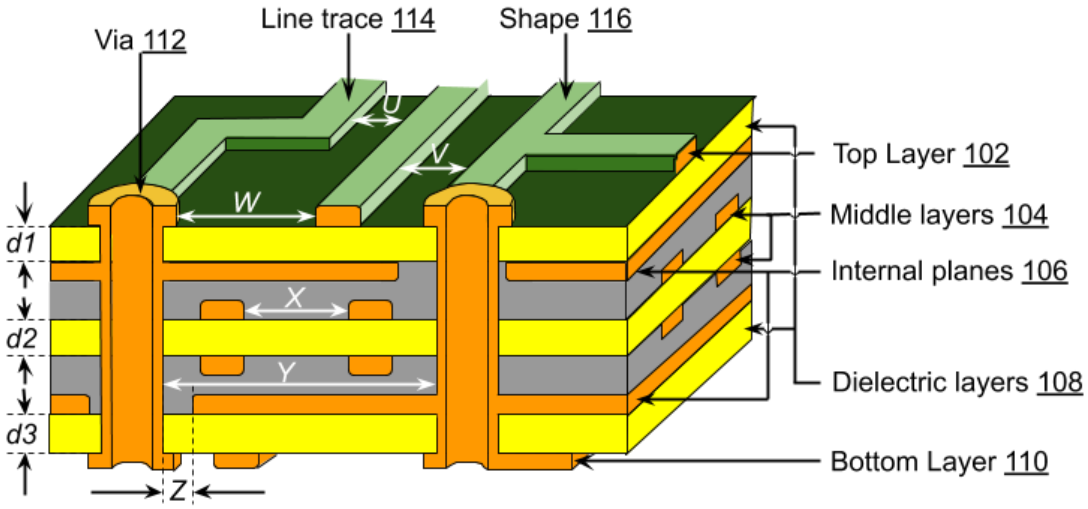


Fig. 1: A multi-layer PCB

As illustrated in Fig. 1, a multi-layer PCB includes multiple conductive layers, including a top layer (102), a bottom layer (110), and one or more internal (or middle) layers (104). A conductive layer comprises computational or signal-processing elements, e.g., pins, bondpads, vias (112), line traces (114), other conductive shapes (116), etc. Types of vias include thru-vias, BB vias, test vias, etc. Types of pins include thru-pins, SMD pins, test pins, etc.

One or more internal conducting planes (106), known as reference planes, establish voltage references, e.g., ground (0 Volts), one or more supply voltages (V_{cc}), etc. A conductive layer or plane is electrically isolated by sandwiching it between dielectric layers (108). The dielectric thicknesses *d1*, *d2*, *d3*, etc. depend on a variety of factors and can vary across the cross-section of the PCB. The distances *U*, *V*, *W*, *X*, *Y*, *Z*, etc. between the various conducting shapes in a conductive layer are known as air-gaps. To optimize signal integrity and minimize cross-talk, air-gaps are designed to satisfy certain constraints, collectively known as the spacing constraint set (SC set). The SC set is typically determined manually by the PCB designer and entered into a computer-aided design (CAD) tool that enforces the spacing constraints.

Calculating, entering, and maintaining an accurate SC set for adequate conductor-to-conductor spacing in PCB designs across a multi-dimensional matrix of possible values is an unwieldy task. The spacing that optimizes signal quality and minimizes cross-talk on a given conductive layer depends on a variety of factors, e.g., dielectric thicknesses in a PCB stack-up, signal technology, voltage, waveform type, data rate, whether the conductors are internal or external to the PCB dielectric, etc.

At present, the entry and maintenance of manually generated or calculated values is onerous and error-prone; designers and engineers frequently enter arrays of worst-case, single-value numbers in the SC sets to simplify their tasks. The result is an approach that does not easily allow for more optimized (smaller) spacing values when designs with higher density are possible, e.g., due to varying dielectric thicknesses in the stack-up. Besides, the present approach of using worst-case values in the SC set is still error-prone.

DESCRIPTION

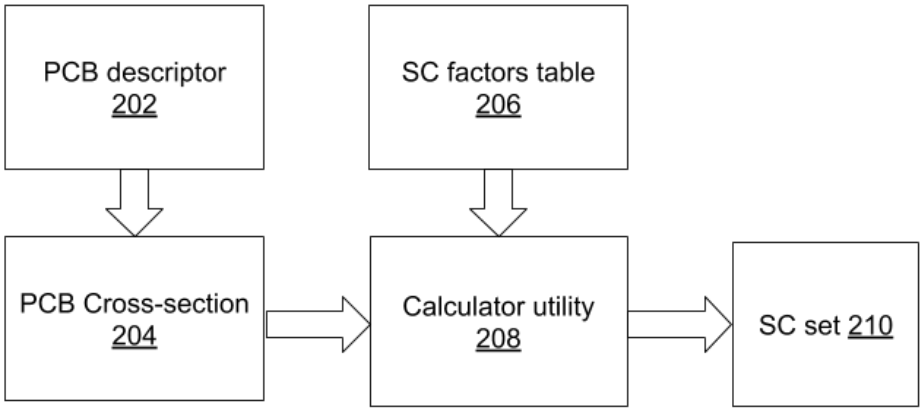


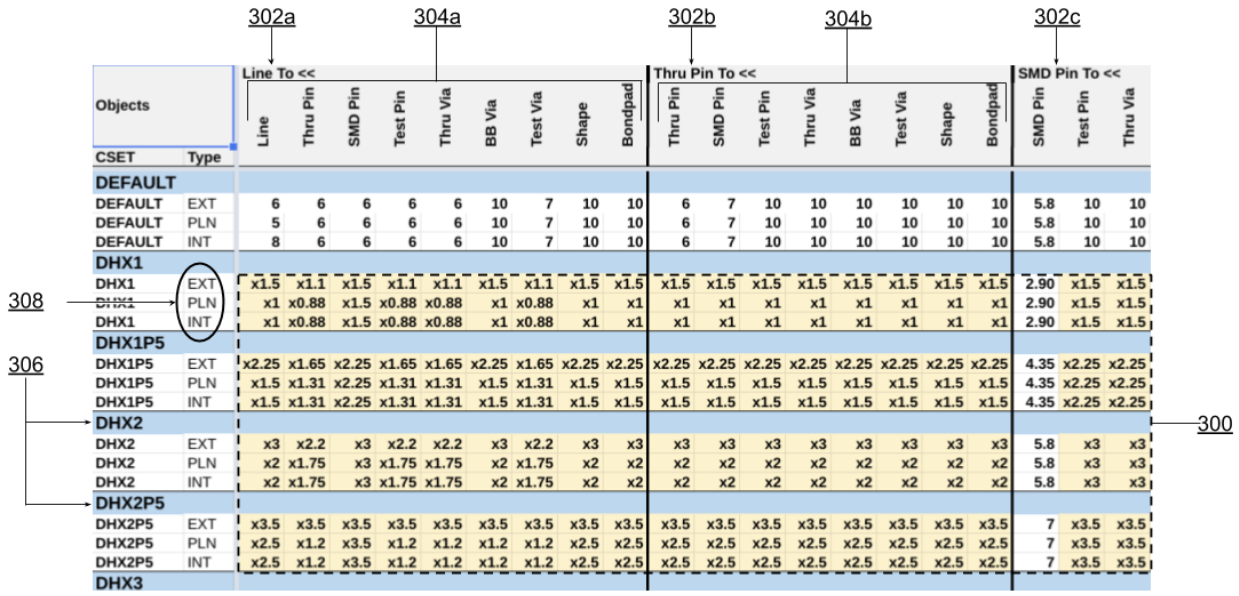
Fig. 2: Automated generation of the SC set

Fig. 2 illustrates automated generation of the SC set, per techniques of this disclosure. A PCB descriptor file (202), typically operable upon by CAD or electronic design automation (EDA) software, specifies the PCB. A cross-section of the PCB (204) that includes the

thicknesses of the various constituent layers of the PCB, e.g., the dielectric thicknesses *d1*, *d2*, *d3*, etc. is extracted from the PCB descriptor file. A spacing constraints factors table (206) is a relatively compact, manually-filled table that comprises multiplicative factors as a function of conductive shape-pairs and the distance of the conductive layer from a reference plane. A calculator utility (208), e.g., a program or a script, receives as input the PCB cross-sections and the SC factors table to generate the SC set (210), e.g., the constraints on the air-gaps *U*, *V*, *W*, *X*, *Y*, *Z*, etc.

The components illustrated in Fig. 2 are described in greater detail below.

Spacing constraints factors table



Objects		Line To <<									Thru Pin To <<								SMD Pin To <<		
CSET	Type	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bondpad	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bondpad	SMD Pin	Test Pin	Thru Via
DEFAULT																					
DEFAULT	EXT	6	6	6	6	6	10	7	10	10	6	7	10	10	10	10	10	10	5.8	10	10
DEFAULT	PLN	5	6	6	6	6	10	7	10	10	6	7	10	10	10	10	10	10	5.8	10	10
DEFAULT	INT	8	6	6	6	6	10	7	10	10	6	7	10	10	10	10	10	10	5.8	10	10
DHX1																					
DHX1	EXT	x1.5	x1.1	x1.5	x1.1	x1.1	x1.5	x1.1	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	2.90	x1.5	x1.5
DHX1	PLN	x1	x0.88	x1.5	x0.88	x0.88	x1	x0.88	x1	x1	x1	x1	x1	x1	x1	x1	x1	x1	2.90	x1.5	x1.5
DHX1	INT	x1	x0.88	x1.5	x0.88	x0.88	x1	x0.88	x1	x1	x1	x1	x1	x1	x1	x1	x1	x1	2.90	x1.5	x1.5
DHX1P5																					
DHX1P5	EXT	x2.25	x1.65	x2.25	x1.65	x1.65	x2.25	x1.65	x2.25	x2.25	x2.25	x2.25	x2.25	x2.25	x2.25	x2.25	x2.25	x2.25	4.35	x2.25	x2.25
DHX1P5	PLN	x1.5	x1.31	x2.25	x1.31	x1.31	x1.5	x1.31	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	4.35	x2.25	x2.25
DHX1P5	INT	x1.5	x1.31	x2.25	x1.31	x1.31	x1.5	x1.31	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	x1.5	4.35	x2.25	x2.25
DHX2																					
DHX2	EXT	x3	x2.2	x3	x2.2	x2.2	x3	x2.2	x3	x3	x3	x3	x3	x3	x3	x3	x3	x3	5.8	x3	x3
DHX2	PLN	x2	x1.75	x3	x1.75	x1.75	x2	x1.75	x2	x2	x2	x2	x2	x2	x2	x2	x2	x2	5.8	x3	x3
DHX2	INT	x2	x1.75	x3	x1.75	x1.75	x2	x1.75	x2	x2	x2	x2	x2	x2	x2	x2	x2	x2	5.8	x3	x3
DHX2P5																					
DHX2P5	EXT	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	x3.5	7	x3.5	x3.5
DHX2P5	PLN	x2.5	x1.2	x3.5	x1.2	x1.2	x1.2	x1.2	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	7	x3.5	x3.5
DHX2P5	INT	x2.5	x1.2	x3.5	x1.2	x1.2	x1.2	x1.2	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	x2.5	7	x3.5	x3.5
DHX3																					

Fig. 3: A spacing constraints factors table

Fig. 3 illustrates a section from an example spacing constraints factors table. As mentioned earlier, a spacing constraints factors table is a relatively compact, manually-filled table that comprises multiplicative factors (300) as a function of conductive shape-pairs and the distance of the conductive layer from a reference plane. A conductive shape-pair is defined as a

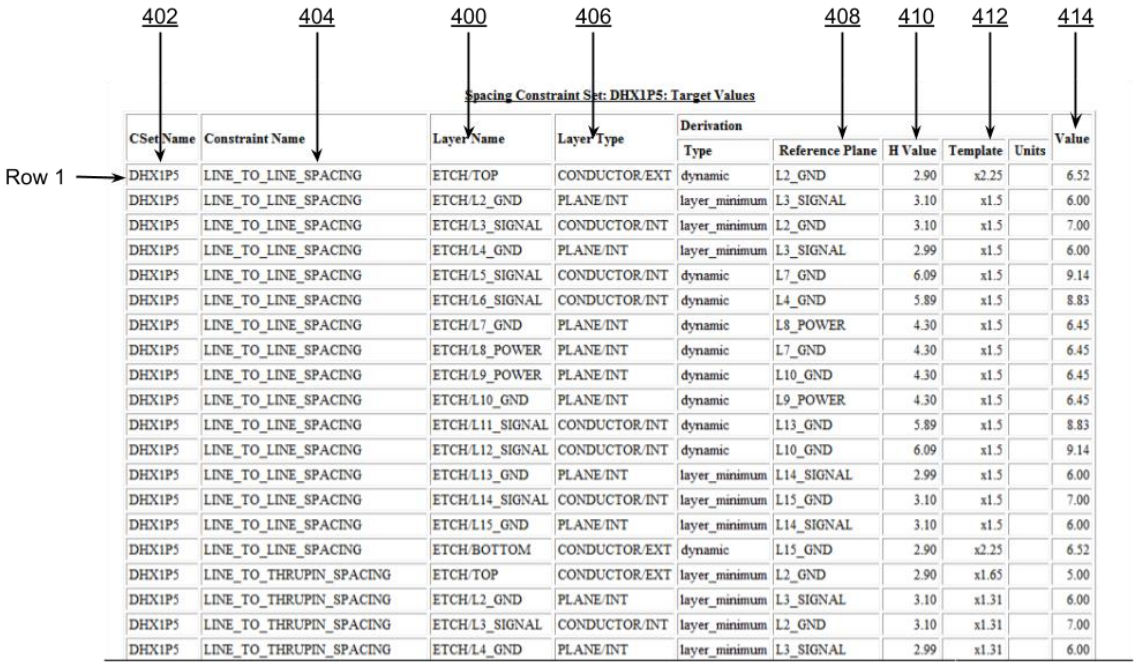
selection of a from-object (302a-c) and a to-object (304a-b). Thus, example shape-pairs can be (line, line), (line, thru pin), (line, SMD pin), (line, bondpad), (thru pin, BB via), (thru pin, test via), etc. Row headings (306) indicate the generally required multiplier of dielectric thickness that achieves adequate spacing. Multipliers vary based on whether the conductive layer is internal to the PCB, external to the PCB, or is a reference plane (308).

Example 1: Reading the DHX2P5 row of the table, the multiplier for a line-to-test-via for an internal layer is found to be 1.2. For a dielectric thickness of 2 mils, the line-to-test-via spacing constraint is 2 mils × 1.2 = 2.4 mils.

Example 2: Reading the DHX2 row of the table, the multiplier for a thru-pin-to-BB-via for an internal layer is found to be 2.0. For a dielectric thickness of 2 mils, the thru-pin-to-BB-via spacing constraint is 2 mils × 2.0 = 4 mils.

Calculator utility

The calculator utility is a script that derives a spacing constraint for a pair of conductive shapes on a conductive layer by multiplying the dielectric thickness of that layer by the multiplicative factor indexed in the spacing constraints factors table.



Spacing Constraint Set: DHX1P5: Target Values

CSet Name	Constraint Name	Layer Name	Layer Type	Derivation Type	Reference Plane	H Value	Template	Units	Value
DHX1P5	LINE_TO_LINE_SPACING	ETCH/TOP	CONDUCTOR/EXT	dynamic	L2_GND	2.90	x2.25		6.52
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L2_GND	PLANE/INT	layer_minimum	L3_SIGNAL	3.10	x1.5		6.00
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L3_SIGNAL	CONDUCTOR/INT	layer_minimum	L2_GND	3.10	x1.5		7.00
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L4_GND	PLANE/INT	layer_minimum	L3_SIGNAL	2.99	x1.5		6.00
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L5_SIGNAL	CONDUCTOR/INT	dynamic	L7_GND	6.09	x1.5		9.14
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L6_SIGNAL	CONDUCTOR/INT	dynamic	L4_GND	5.89	x1.5		8.83
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L7_GND	PLANE/INT	dynamic	L8_POWER	4.30	x1.5		6.45
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L8_POWER	PLANE/INT	dynamic	L7_GND	4.30	x1.5		6.45
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L9_POWER	PLANE/INT	dynamic	L10_GND	4.30	x1.5		6.45
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L10_GND	PLANE/INT	dynamic	L9_POWER	4.30	x1.5		6.45
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L11_SIGNAL	CONDUCTOR/INT	dynamic	L13_GND	5.89	x1.5		8.83
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L12_SIGNAL	CONDUCTOR/INT	dynamic	L10_GND	6.09	x1.5		9.14
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L13_GND	PLANE/INT	layer_minimum	L14_SIGNAL	2.99	x1.5		6.00
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L14_SIGNAL	CONDUCTOR/INT	layer_minimum	L15_GND	3.10	x1.5		7.00
DHX1P5	LINE_TO_LINE_SPACING	ETCH/L15_GND	PLANE/INT	layer_minimum	L14_SIGNAL	3.10	x1.5		6.00
DHX1P5	LINE_TO_LINE_SPACING	ETCH/BOTTOM	CONDUCTOR/EXT	dynamic	L15_GND	2.90	x2.25		6.52
DHX1P5	LINE_TO_THRUPIN_SPACING	ETCH/TOP	CONDUCTOR/EXT	layer_minimum	L2_GND	2.90	x1.65		5.00
DHX1P5	LINE_TO_THRUPIN_SPACING	ETCH/L2_GND	PLANE/INT	layer_minimum	L3_SIGNAL	3.10	x1.31		6.00
DHX1P5	LINE_TO_THRUPIN_SPACING	ETCH/L3_SIGNAL	CONDUCTOR/INT	layer_minimum	L2_GND	3.10	x1.31		7.00
DHX1P5	LINE_TO_THRUPIN_SPACING	ETCH/L4_GND	PLANE/INT	layer_minimum	L3_SIGNAL	2.99	x1.31		6.00

Fig. 4: Calculations performed by the calculator utility

Fig. 4 illustrates an example of the calculations performed by the calculator utility to arrive at a spacing constraint. The notation for the constraint set, DHX1P5 (402), signifies that the generally required multiplier of dielectric thickness to achieve adequate spacing is 1.5. Focusing on row 1, the layer under consideration, ETCH/TOP (400) has reference plane L2_GND (408). Indexing into the spacing constraints factors table, the multiplicative factor for line-to-line spacing (404) for an external (406) DHX1P5 layer is 2.25 (412). The dielectric thickness (410) is 2.90 mils. Therefore, the spacing constraint for line-to-line spacing on this layer is calculated as 2.90 × 2.25 = 6.52 mils (414). During the course of design, if a designer places two lines less than 6.52 mils of each other, then the design tool throws an error. In a similar manner, the calculator utility computes the spacing constraint at other rows, e.g., for other conductive shape-pairs at other PCB layers.

Spacing constraints set

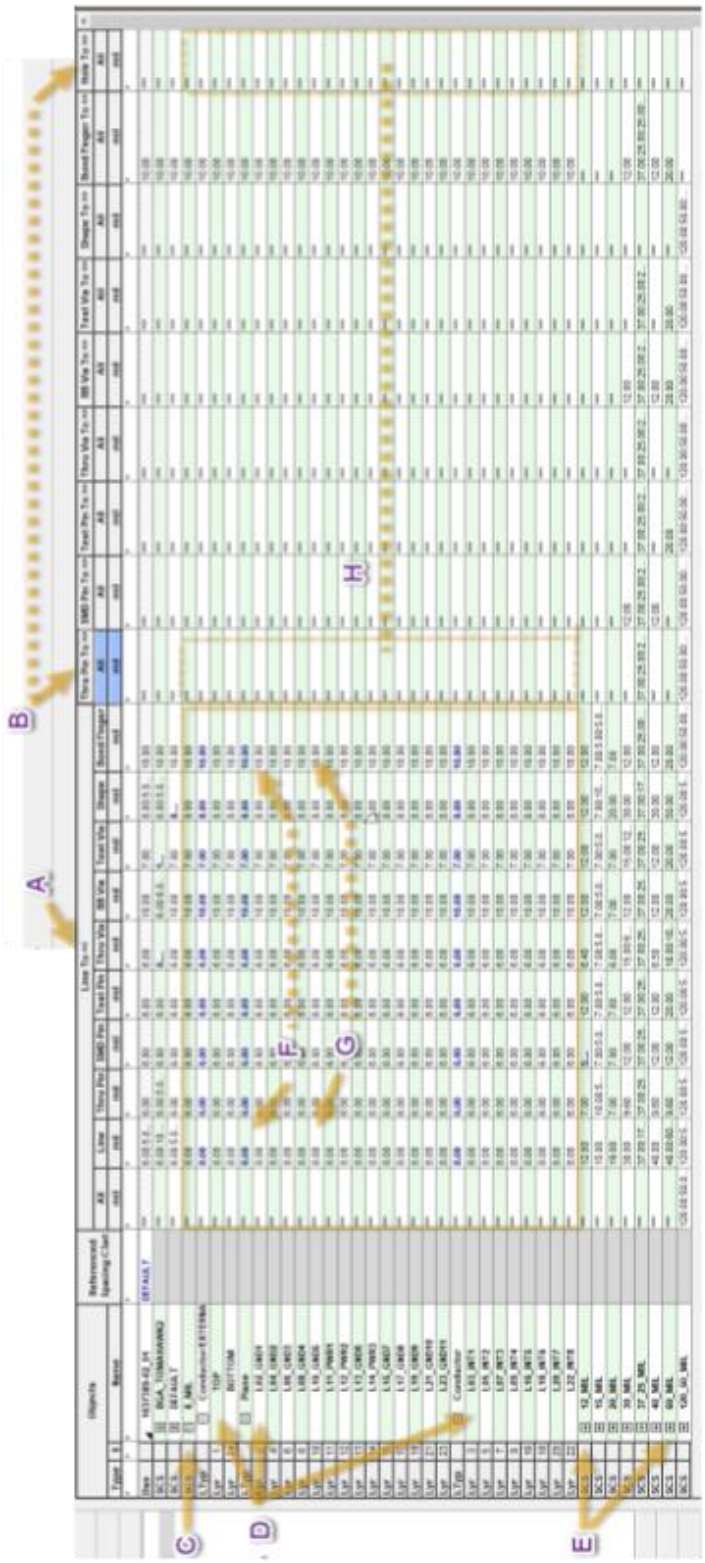


Fig. 5: The spacing constraints set

The output of the calculator utility is the spacing constraints set, an example of which is illustrated in Fig. 5. As mentioned before, the SC set specifies minimum spacings for a pair of conducting shapes at a conductive layer of a multi-layer PCB. The SC set, transformed in format to be compatible to a CAD tool, is input to the CAD tool, which enforces the constraints specified in the SC set. Referring to Fig. 5, the annotated regions of the SC set are described in the table below.

A:	A group of conductive-pair spacing constraints, e.g., line-to-line, line-to-via, line-to-thru'pin, etc.
B:	Remaining groups of conductive-pair spacing constraints, e.g., thru'pin-to-others, SMD-to-others, etc. A group includes one complimentary value of each other group, e.g., line-to-thru'pin in the first group is the same as thru'pin-to-line in the second group. For illustration, these groups are shown collapsed. When expanded, they appear similar to the first group.
C:	Spacing constraint set (SC set) name. 'DEFAULT' is the minimum SC set required. SC sets comprise hierarchy (layer set types, then individual layers).
D:	Within each SC set are PCB layers, e.g., outer (top/bottom), inner plane (L02...L23), inner conductor (L03...L22), etc.
E:	Other SC sets defined in this design; each with a full complement of layers and conductive-pair constraints.
F:	Spacing constraint value. If in bold font, the value has been set directly in this cell; if not it has been inherited from higher up in SC set hierarchy.
G:	Spacing constraint value. If in bold font, the value has been set directly in this cell; if not it has been inherited from higher up in SC set hierarchy.
H:	Remaining constraints for conductive pairs.

Table: Annotated regions of the SC set

In this manner, the techniques of this disclosure render an accurate and understandable representation of the full *n*-axis matrix of values in the spacing-constraints space by flattening

the matrix and projecting it into a lower-dimensional space that clarifies and distills it. The physics of PCB design engineering (edge rates, fringe fields, cross-talk victims and aggressors, etc.) defines many of the values, and the design tool presents the rest (board structure, entity types, relationships, etc.). The techniques simplify and standardize the user interface, and bridge the gap between an unmanageable interface and a desired outcome for working design geometry.

CONCLUSION

This disclosure describes techniques to automatically calculate spacing constraints within a multi-layer printed circuit board given dielectric thicknesses, conducting shape-pairs, and other parameters. The techniques enable design of efficient, high-density PCBs with excellent signal integrity.