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November 2019

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N/A, "Reconfigurable power delivery network for multi-chip packages", Technical Disclosure Commons, (November 14, 2019)

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Reconfigurable power delivery network for multi-chip packages

ABSTRACT

A multi-chip package has a number of processor cores or integrated circuits (ICs). To optimize performance and power consumption, different ICs can be operated at different voltages and frequencies (dynamic voltage and frequency scaling, or DVFS). DVFS is enabled by the presence of independently regulated power rails supplying an IC or a group of ICs. However, distinct power rails within a multi-chip package result in a fragmented power delivery network (PDN), which in turn causes large voltage drops that compromise performance and reliability. Per the techniques of this disclosure, critical power rails, which are relatively few in number, are distributed globally, e.g., throughout the package. Less critical, or local, power rails switch to one of the global power rails depending on voltage level appropriate to the local power rail. The techniques result in DVFS with lowered cost and a more robust PDN with smaller voltage drops, better performance, and higher reliability.

KEYWORDS

- Multi-chip package (MCP)
- Power distribution network (PDN)
- Power delivery network (PDN)
- Reconfigurable PDN
- Dynamic voltage and frequency scaling (DVFS)
- Dynamic clock and voltage scaling (DCVS)
- Power rail

BACKGROUND

Power rail →	Core		SRAM		TOP	
Mode ↓	Voltage	Frequency	Voltage	Frequency	Voltage	Frequency
Turbo	0.95 V	1.2 GHz	0.85 V	1.0 GHz	1.0 V	1.0 GHz
Nominal	0.90 V	1.0 GHz	0.80 V	0.9 GHz	0.95 V	0.9 GHz
SVS	0.80 V	0.9 GHz	0.70 V	0.8 GHz	0.90 V	0.8 GHz
Low SVS	0.70 V	0.8 GHz	0.60 V	0.7 GHz	0.85 V	0.7 GHz

Table 1: Dynamic voltage and frequency scaling in a multi-chip package

A multi-chip package has a number of processor cores or integrated circuits (IC). The ICs can operate in differing modes that optimize or trade off performance and power consumption. For example, Table 1 shows four modes (turbo, nominal, SVS, and low SVS) for each of three power rails (core, SRAM, TOP) in a multi-chip package. Upper rows in the table correspond to higher performance and power consumption. During operation, it is possible, for example, that the core power rail is supplied with a higher supply voltage and frequency (for maximum performance), while the SRAM power rail is supplied with a lower voltage and frequency (to reduce power consumption), while the TOP power rail is supplied with an intermediate voltage and frequency.

The framework for supplying a constituent IC with its own voltage and frequency for the purpose of optimizing or trading off performance and power consumption is known as dynamic voltage and frequency scaling (DVFS). Under DVFS, the voltage (and frequency) combination

for the set of constituent ICs is optimized based on the workload and power consumption targets for each IC. DVFS is also known as DCVS (dynamic clock and voltage scaling).

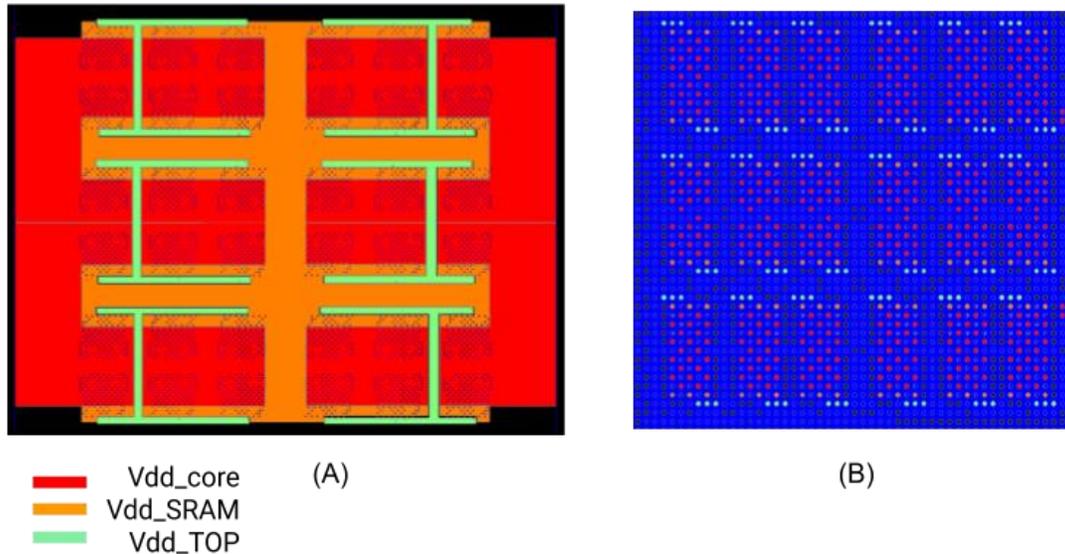


Fig. 1: (A) Power rails in a multi-chip package (B) Corresponding voltages at the ball-grid array

DVFS is enabled by the presence of independently regulated power rails (also known as voltage islands or domains) for an IC or group of ICs. This is illustrated in Fig. 1A, which shows power rails of a multi-chip package in different colors. Fig. 1B shows the voltages for the power rails as they appear at the ball-grid array. However, distinct power rails within a multi-chip package result in a fragmented power delivery network (PDN), which in turn causes large voltage drops that compromise performance and reliability. A fragmented PDN also results in an increased resistance and inductance, causing greater heat loss, and hinders the sharing of on-chip, decoupling capacitances across rails, further contributing to unacceptably large voltage drops. Multiple power rails also entail additional components and design effort, not only within the chip but also on the board that hosts the chip.

DESCRIPTION

Per the techniques of this disclosure, critical power rails, which are relatively few in number, are distributed globally, e.g., throughout the package. Less critical, or local, power rails switch to one of the global power rails depending on voltage set point (level) appropriate to the local power rail.

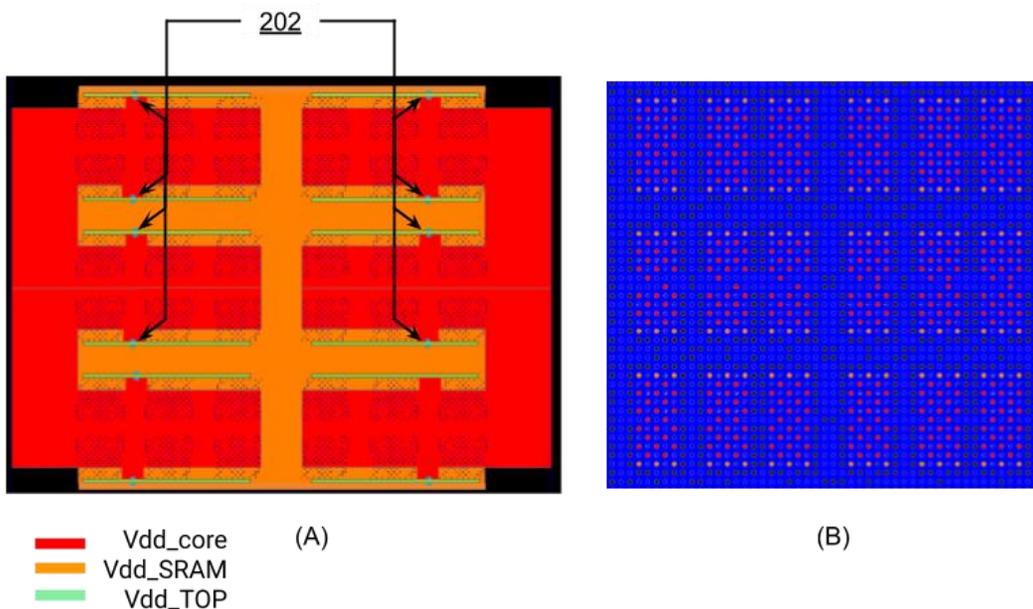


Fig. 2: Reconfigurable power delivery network (A) Power rails (B) Ball-grid array

Fig. 2 illustrates reconfigurable power delivery network, per techniques of this disclosure. As illustrated by the example of Fig. 2A, one or more power rails, e.g., the green power rail, is shrunk in extent, e.g., localized to specific regions of the multi-chip package. The remaining power rails, e.g., the red and orange rails, remain globally distributed. Switches (202) are installed throughout the localized power rail that enable its connection to one of the global power rails. In this manner, the localized (green, TOP) power rail can be set to one of the voltages on the global rails (red, orange). The switches can be discrete and placed on-package, e.g., they can have die-side placement or be placed in gaps between die-lets. The switches can also be

integrated into the die, e.g., as an array of CMOS (NMOS or PMOS) transistors. Fig. 2B shows the voltages at the ball-grid array, which are now of just two colors (compare with Fig. 1B).

Mode	Vdd: Core	Vdd: SRAM	Vdd: TOP
Turbo	0.85V	1V	1 or 0.85V
Nominal	0.8V	0.95V	0.8 or 0.95V
SVS	0.7V	0.9V	0.7 or 0.9V
Low SVS	0.6V	0.85V	0.6 or 0.85V

Table 2: The TOP power rail can be dynamically reconfigured to connect to the voltage of either the core or the SRAM power rails

Table 2 illustrates dynamic reconfigurability of the power distribution network, per techniques of this disclosure. The TOP power rail can be reconfigured to connect to the voltage of either the core power rail or the SRAM power rail. For example, if both core and SRAM power rails are in turbo mode then the TOP power rail can be set to either 0.85 V or 1 V. If the core power rail is in low-SVS mode (0.6 V) and the SRAM power rail is in turbo mode (1 V), then the TOP power rail can be set to either 1 V or 0.6 V. The voltage that the TOP power rail is set to depends on its workload and power consumption target.

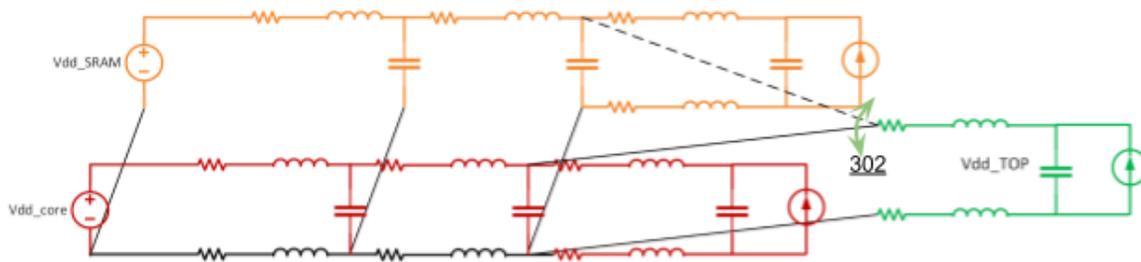


Fig. 3: Electrical schematic for reconfigurable power delivery network

Fig. 3 illustrates an electrical schematic for reconfigurable power delivery network, per

techniques of this disclosure. A switch (302) throws the green (TOP) power rail between the red (core) power rail and the orange (SRAM) power rail. When connected to any one global (red or orange) circuit, the local (green) power rail shares the decoupling capacitances of the global circuit, thereby reducing the component count.

In this manner, the techniques of this disclosure enable a fewer number of power rails to be globally distributed, resulting in reduced costs, e.g., fewer package components, PCB components, on-chip and on-board power rails, board layers, etc.; a larger amount of shared resources available on the package and PCB, e.g., a larger on-die, decoupling capacitance due to the merged power rails; and a more robust power delivery network. Dynamic voltage and frequency scaling (DVFS), with its concomitant power-versus-performance trading-off capability is supported. However, fewer power rails, which amount to a type of metal-resource consolidation, not only lower cost, but also result in a more robust PDN with smaller voltage drops, better performance, and higher reliability.

CONCLUSION

Per the techniques of this disclosure, the critical power rails of a multi-chip package, which are relatively few in number, are distributed globally, e.g., throughout the package. Less critical, or local, power rails switch to one of the global power rails depending on voltage level appropriate to the local power rail. The techniques result in dynamic voltage and frequency scaling (DVFS) with lowered cost and a more robust power distribution network (PDN) with smaller voltage drops, better performance, and higher reliability.