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Temperature Controlled Stacked Board Cavity

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Abstract:

This publication describes techniques and apparatuses that decrease the temperature variation in a cavity created by an interposer that stacks two or more boards inside a smartphone. When operating electrical components, heat generation is inevitable. A way to minimize temperature variation is by embracing and managing a safe rise in temperature in and/or around the electrical components inside the cavity of the interposer. A safe rise in temperature may be a temperature between +25°C and +85°C (*e.g.*, +55°C). That way, when the smartphone shifts from an idle state to normal operation, the cavity of the interposer and the electrical components inside the cavity do not experience a large temperature variation—the cavity is pre-warmed. Less temperature variation enables the smartphone to use less complex software and lookup tables that are limited to one temperature (*e.g.*, +55°C) instead of a wide range of temperatures, such as from -40°C to +85°C. Limiting temperature variation by keeping the cavity of the interposer above room temperature and below the maximum temperature offers consistent smartphone performance, better space utilization, and decreased manufacturing and/or operational cost.

Keywords:

Interposer, stacked boards, multiple boards, printed circuit board, PCB, board cavity, interposer cavity, envelope tracking, temperature control, temperature variation, envelope tracking, lookup table, shaping table.

Background:

An original device manufacturer (ODM) of a smartphone often uses interposer architectures to stack two or more boards, such as printed circuit boards (PCBs) and flexible PCBs (FPCBs), to optimize space usage. A PCB can include two, three, four, or more, layers that help route and electrically isolate signal traces (*e.g.*, clock, input, output) and planes (*e.g.*, ground plane, power plane) that are embedded in or on the PCB. In addition, the ODM may embed multiple chips, transceivers, filters, power amplifiers, passive electrical elements, active electrical elements, processors, and so forth, collectively "electrical components," on top and/or on the bottom of each PCB.

Under normal operating conditions, each electrical component embedded on top and/or on the bottom of each PCB generates thermal energy (heat) due to power loss. The smartphone needs to mitigate this heat. Mitigating heat when using a single (unstacked) board is easier than mitigating heat when using an interposer with two or more stacked boards. When using a single board, the electrical components are often exposed to air, which helps cool down the electrical components. In contrast, mitigating heat when using an interposer with two or more boards stacked on the top, on the bottom, and/or adjacent to each other, is more challenging. The interposer may be a NEMA-grade glass-reinforced epoxy laminate material (FR4) or a more exotic material. Regardless of the material used in the interposer, the stacking of two or more boards creates a cavity that can trap the heat generated by the electrical components inside the cavity.

Trapped heat inside the cavity of the interposer can cause performance issues. To this end, many smartphones use temperature sensors, cooling circuits, exotic thermal-interface materials, active cooling integration (*e.g.*, micro fans), heat sinks (*e.g.*, metal fill, metal plates), elaborate and costly PCB and interposer designs, and other techniques and apparatuses, to monitor temperature

and cool down the electrical components. Note that some of the techniques and apparatuses to help cool down the electrical components may be active (require power) or may be passive (do not require power). Also, some of the techniques and apparatuses to help cool down the electrical components may be accomplished using conduction, convection, and/or radiation principles. Techniques and apparatuses using active, passive, conduction, convection, and/or radiation to cool down the electrical components may require energy, space, increased cost, or all the above. Further, even when the ODM of the smartphone is willing and able to spend the required resources to help cool down the electrical components, the smartphone may fail to decrease the temperature in and/or around the electrical components in a short enough time, causing electrical performance issues due to temperature variation.

Therefore, it is desirable to have a technological solution that can minimize the temperature variation in the cavity of an interposer.

Description:

This publication describes techniques and apparatuses that decrease the temperature variation in a cavity created by an interposer that stacks two or more boards. When operating electrical components, heat generation is inevitable. Conventional techniques and apparatuses utilized to handle temperature variations often struggle to address the issues resulting from temperature variation. A way to minimize temperature variation is by embracing and managing a safe rise in temperature in and/or around the electrical components inside the cavity of the interposer. A safe temperature for an electronic component may be specified in global standards for the microelectronics industry promulgated by JEDEC®. For example, JEDEC® standards may specify that certain electronic components can safely operate between -40°C and +85°C, where

+25°C is considered to be room temperature. Therefore, a safe rise in temperature may be a temperature between +25°C and +85°C (*e.g.*, +55°C).

Figure 1 helps demonstrate an example of an interposer board cavity.

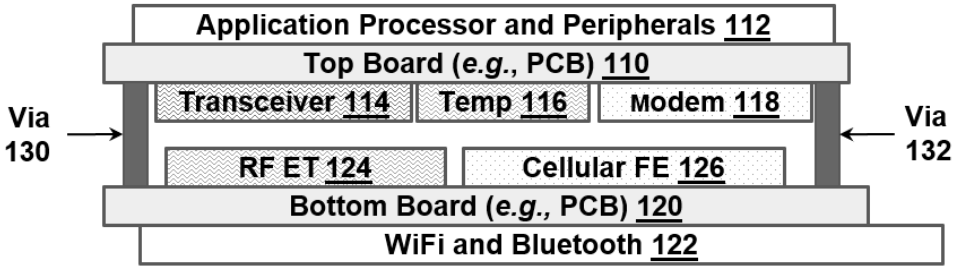

Figure 1

Figure 1 illustrates an example of an interposer design that stacks a top board 110 above a bottom board 120 utilizing multiple via structures, such as via 130 and via 132 (not all via structures are illustrated in Figure 1). The top board 110 and the bottom board 120 are multi-layer boards (*e.g.*, PCBs). The top board 110 has an application processor and peripheral circuitry 112 embedded above the top board 110, and a transceiver 114, a temperature control circuit 116, and a modem 118 embedded below the top board 110. The bottom board 120 has a radio frequency envelope tracking (RF ET) 124 circuit(s) and a cellular front end (cellular FE) 126 circuit embedded above the bottom board 120 and circuits that support communication protocols, such as WiFi™ and Bluetooth™ 122, embedded below the bottom board 120.

The performance of the electrical components is affected by multiple factors, such as variations in manufacturing processes, voltage, frequency, and temperature. The ODM of the smartphone often designs around these factors. The various electrical components perform an array of high-speed, power-hungry, and complex computations causing the electrical components to generate heat and the temperature to rise in and/or around the electrical components. When the electrical components are in an idle state, heat dissipates, and the temperature in and/or around the

electrical components decrease. Increases and decreases in temperature (temperature variation) bring a new set of challenges due to the inability of the smartphone to mitigate temperature variation fast enough. To this end, the smartphone may utilize lookup tables (LUTs) to change the input voltage to an electrical component depending on the temperature and the frequency that the electrical component operates. Note that LUTs sometimes are referred to as shaping tables. The heat generated by operating the transceiver 114, the modem 118, the RF ET 124, and the cellular FE 126 can be trapped in the cavity created between the top board 110 and the bottom board 120. The transceiver 114 may perform several functions, such as up-convert and/or down-convert baseband in-phase/quadrature (I/Q) signals to radio frequencies (RF). The modem 118 performs baseband and I/Q digital signal processing. Using LUTs, the RF ET 124 adjusts the voltages of the cellular power amplifiers (PAs) depending on the operating frequency and the temperature of the PAs. Note that LUTs are used in the cellular FE 126 containing PAs, filters, switches, low noise amplifiers (LNAs), and passive electrical components (*e.g.*, resistors, capacitors, inductors) that behave differently under different temperatures. For example, as the temperature increases, the resistance of a resistive element also increases. Capacitance variation due to temperature variation is particularly challenging and costly to manage, which will become clearer in later descriptions.

Figures 2A, 2B, 2C, and 2D help illustrate conventional complex codebooks created over a wide temperature range (-40°C to +85°C) that are used to compensate for this temperature variation in the dynamics of the PAs. Dynamics of the PA include signal parameters, such as S_{21} that stands for the forward voltage gain (often referred to as the small-signal gain), P_{1dB} that stands for the output power when the PA is at the one decibel (1 dB) compression point, and P_{sat} that stands for the output power when the PA operates in the saturation region.

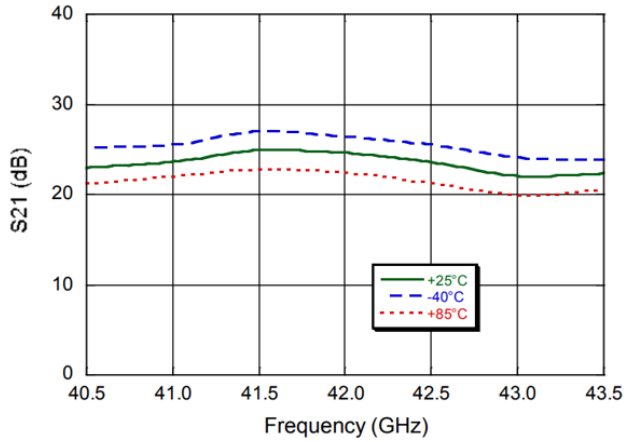

Figure 2A

Figure 2A illustrates the parameter S_{21} in dB of an example PA over a frequency range between 40.5 gigahertz (GHz) and 43.5 GHz. Additionally, Figure 2A illustrates how the parameter S_{21} differs between a minimum temperature -40°C, room temperature +25°C, and a maximum temperature +85°C.

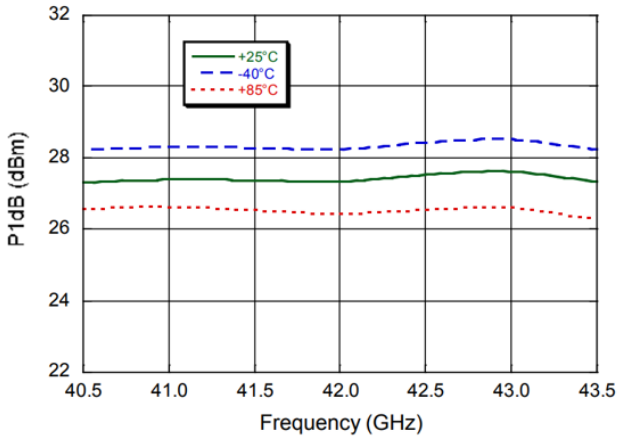

Figure 2B

Figure 2B illustrates the parameter P_{1dB} in decibel-milliwatts (dB_m) over the same frequency range between 40.5 GHz and 43.5 GHz. Similar to Figure 2A, Figure 2B illustrates how the parameter P_{1dB} differs between the minimum temperature -40°C, room temperature +25°C, and the maximum temperature +85°C.

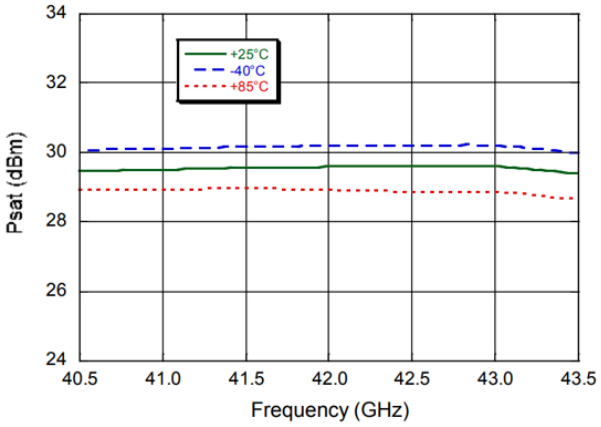

Figure 2C

Figure 2C illustrates the parameter P_{sat} in dB_m over the same frequency range between 40.5 GHz and 43.5 GHz. Similar to Figure 2A and Figure 2B, Figure 2C illustrates how the parameter P_{sat} differs between the minimum temperature -40°C, room temperature +25°C, and the maximum temperature +85°C.

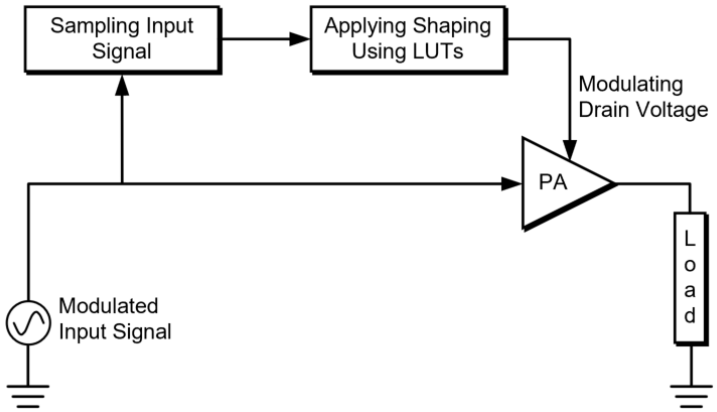

Figure 2D

Figure 2D illustrates how conventional smartphones utilize the data illustrated in Figure 2A, Figure 2B, and Figure 2C to compensate for temperature variation in the dynamics of the PAs. The ODM of the smartphone employs LUTs that are constructed by modeling and/or pre-characterizing a select number of smartphones. The LUTs are used to compensate for temperature

variation in an envelope tracking system. The illustrated complex LUTs also require complex software that can support the LUTs. As is illustrated in the example of Figure 2D, to operate the PA across a wide temperature variation, the supporting software needs to first enable sampling of a modulated input signal to the PA. Then, the supporting software applies shaping using complex LUTs to properly modulate the drain voltage of the PA, which drives a load. To complicate matters even further, the load itself may also change electrical characteristics (*e.g.*, a change in resistance, capacitance, and/or inductance) due to temperature variation. Note that the example in Figure 2D does not address the change in the electrical characteristics of the load. Further, the utilization of complex LUTs and complex software does not guarantee that the software references the correct LUT during a quick rise in temperature, such as when the smartphone progresses from an idle state to a normal operating condition.

To address the issues described with respect to Figure 1, Figure 2A, Figure 2B, Figure 2C, and Figure 2D, the techniques and apparatuses described herein reduce temperature variation by using the ability of the interposer cavity to limit temperature variation. Given that a rise in temperature above room temperature is inevitable under normal operating conditions, and given that the cavity of the interposer traps the heat generated during normal operating conditions, the smartphone can stabilize the temperature under all operating conditions. To do so, when the smartphone is in an idle state, the smartphone can run wait cycles through the electrical components and utilize the dissipated heat to quickly (*e.g.*, five seconds) and safely increase the temperature above room temperature inside the interposer cavity. That way, when the smartphone shifts from an idle state to normal operation, the cavity of the interposer and the electrical components inside the cavity do not experience a large temperature variation—the cavity is pre-warmed. Less temperature variation enables the smartphone to use less complex software and

LUTs because the shaping tables are limited to one temperature (*e.g.*, +55°C) instead of a wide range of temperatures, such as between -40°C and +85°C. The smartphone can use energy from a battery of the smartphone to run "wait cycles" in the electrical components inside the interposer cavity. Alternatively or in addition to, the smartphone can repurpose or divert heat generated from electrical components outside the cavity of the interposer and channel the heat inside the cavity of the interposer. Limiting temperature variation inside the cavity of the interposer by purposefully increasing the temperature above room temperature is easier than limiting the temperature variation inside the cavity of the interposer by decreasing the temperature inside the cavity of the interposer because the cooling process takes considerably more time and/or resources (*e.g.*, heat sinks, micro fans, energy to run active cooling). It is worth noting that the described techniques and apparatuses purposefully and safely increase the temperature inside the cavity of the interposer and do not increase the temperature in electrical components elsewhere in the smartphone nor outside the smartphone.

Limiting temperature variation by keeping the cavity of the interposer above room temperature and below the maximum temperature offers consistent smartphone performance, better space utilization, and decreased cost. Also, the smartphone can safely use a variety of capacitors, as is illustrated in Figure 3.

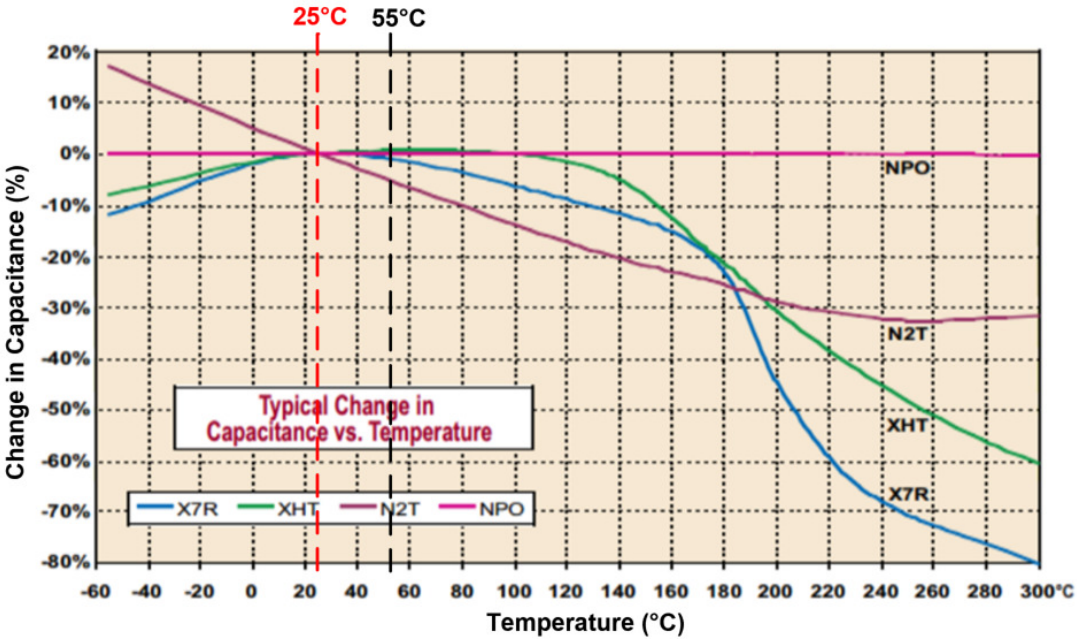

Figure 3

Figure 3 illustrates a change in the percentage of capacitance in four capacitors with dielectric codes NPO, N2T, XHT, and XR7, as a function of a change in temperature from room temperature (+25°C). The capacitor with the dielectric code NPO is a Class I capacitor and displays little capacitance variation across a wide range of temperatures. NPO Class I capacitors, however, can be expensive and/or large. By keeping the cavity inside the interposer above room temperature and below the maximum temperature, the smartphone can utilize higher density and smaller X7R Class II, or even Class III, capacitors in RF circuits. Smaller and less costly capacitors enable the smartphone to utilize resources better and still offer good performance.

In conclusion, limiting temperature variation by keeping the cavity of the interposer above room temperature and below the maximum temperature offers a consistent performance of the smartphone, better space utilization, and decreased manufacturing and/or operational cost.

References:

[1] Patent Publication: US20130285739A1. Methods, apparatus and system to support large-scale micro-systems including embedded and distributed power supply, thermal regulation, multi-distributed sensors and electrical signal propagation. Priority Date: September 7, 2010.

[2] Patent Publication: US20190074818A1. Transmit-receive delay element apparatus, method, and applications. Priority Date: March 17, 2016.

[3] Patent Publication: WO2012031362A1. Methods, apparatus and system to support large-scale micro- systems including embedded and distributed power supply, thermal regulation, multi-distributed-sensors and electrical signal propagation. Priority Date: September 7, 2010.

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