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Adapter With Power Allocable Among Multiple Output Ports

Chao Fei

Honggang Sheng

Doug Osterhout

Srikanth Lakshmikanthan

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ABSTRACT

Multi-output chargers typically limit the maximum power per output port. This disclosure describes a low cost, low complexity, multi-output charger/adapter that can allocate a total available power smoothly among multiple output ports.

KEYWORDS

- Power adapter
- Charger
- Multi-output adapter
- Flyback transformer
- Power regulator
- Galvanic isolation

BACKGROUND

Multi-output chargers (adapters) are in widespread use. A popular use is to simultaneously charge a mobile device and a laptop or other device. Multi-output chargers currently limit the maximum power per output port. For example, a 40-Watt, dual-output, USB-C charger limits the power output per port to 20 Watts. A user that charges a laptop using one of the ports finds the charging to be slow, even if the other output port is not charging another device. A charger that allocates all forty watts to the one port currently under use makes for a better user experience.

Although there have been attempts at designing multi-output chargers that are capable of delivering the total available power at each output port, such chargers have large end-stages and complex, software-controlled, multi-stage architectures, both of which increase cost and size.

DESCRIPTION

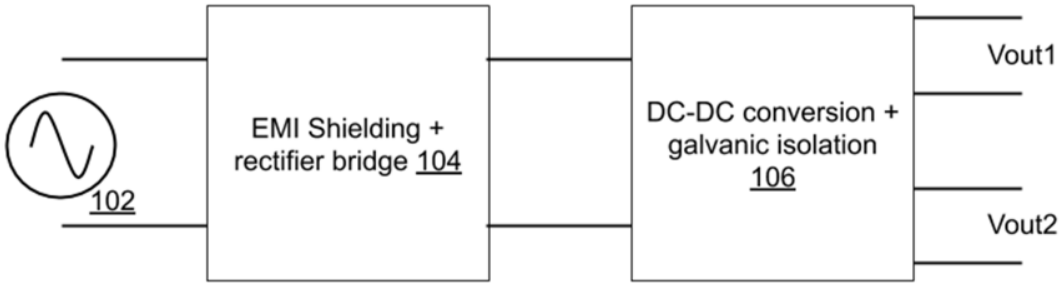

Fig. 1: Block diagram of a multi-output power adapter

Fig. 1 illustrates a block diagram of a multi-output power adapter, per techniques of this disclosure. An AC source (102) feeds into a rectifier bridge (104) that also serves to shield against electromagnetic interference (EMI). The rectified signal is processed by a multi-output DC-DC conversion stage (106) that also serves to provide galvanic isolation. The DC-DC conversion stage provides multiple, independently regulable outputs. For simplicity, two outputs, Vout1 and Vout2, are shown; however, the techniques described herein can be used for an arbitrary number of outputs.

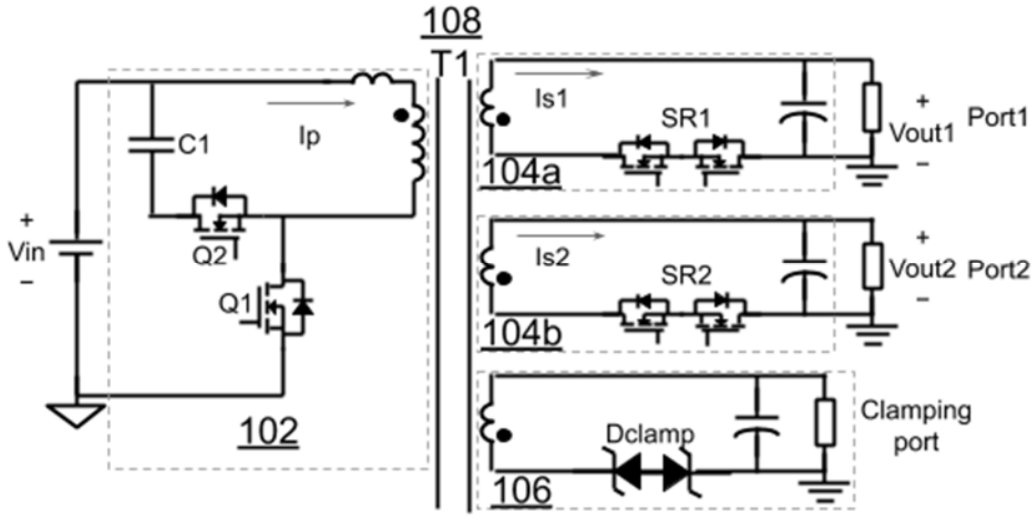

Fig. 2: Circuit schematic of a multi-output DC-DC converter

The DC-DC conversion stage is illustrated in greater detail in Fig. 2. A flyback transformer core T1 (108) has a primary circuit (102) that accepts as input a rectified signal Vin. The flyback transformer has several secondary circuits (104a-b), each corresponding to an isolated, independent, output port. While Fig. 2 illustrates two secondary circuits and corresponding outputs (port1, port2), the described circuit is generalizable to an arbitrary number of isolated, independent outputs. A clamping circuit (106) on the secondary side of the transformer prevents the unwanted build-up of large voltages in the secondary circuits during start-up or under transient conditions.

The primary circuit is controlled by two switches, Q1 and Q2, whose on-off periods are complementary to each other, Q1 serving as the main power switch. Alternatively, the gate signal of Q2 can be on for a short period of time when Q1 is off. An alternative circuit topology is to replace Q2 and the capacitor C1 by a passive clamping circuit.

Each secondary circuit is controlled independently, e.g., without cross-regulation, by back-to-back FETs. For example, secondary circuit 104a is controlled by back-to-back FET SR1 and secondary circuit 104b by back-to-back FET SR2. Following modes of control are provided, each described in greater detail below.

- Discontinuous conduction mode (DCM)
- Critical conduction mode (CRM)
- Combined DCM-CRM mode

Discontinuous conduction mode

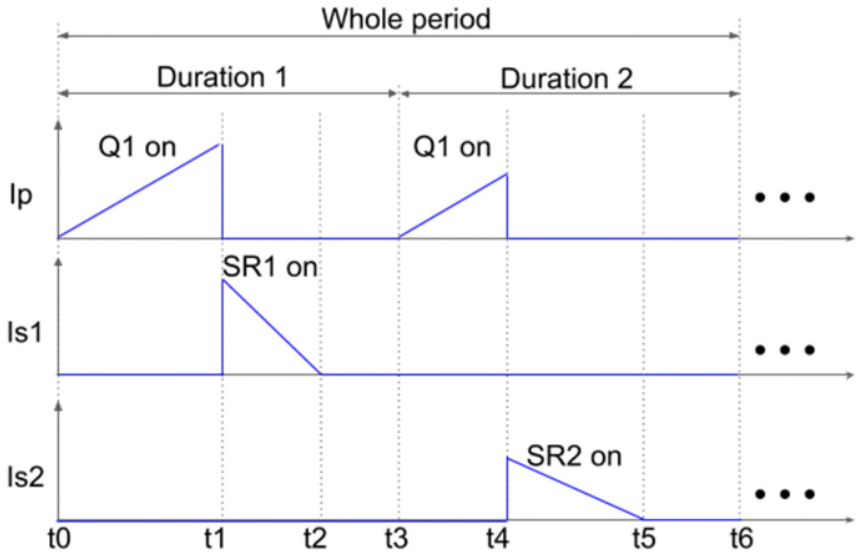

Fig. 3: Control waveforms for discontinuous control mode

Fig. 3 illustrates control waveforms for discontinuous control mode (DCM). Under DCM, the primary circuit current (Ip) and the secondary circuit currents (Is1, Is2) are controlled using their respective switches (Q1, Q2, SR1, SR2) in the manner illustrated in Fig. 3. The waveform pattern, shown in Fig. 3 over a single whole period, is repetitive. A period comprises as many durations (e.g., duration 1, duration 2) as output ports. The ratios of the durations within a whole period determine the power allocations to the output ports. For example, a large duration-1 to duration-2 ratio causes the bulk of the total available power to flow to output port 1.

Within duration 1, during time interval [t0, t1], the primary switch Q1 is on (and its complementary switch Q2 is off), and secondary switches SR1, SR2 are off, such that the primary current Ip builds linearly. At time t1, Q1 is turned off and switch SR1 of the first secondary circuit is turned on, such that the energy in the primary circuit is transferred to the first

secondary circuit, leading to a current Is1 (as shown) in the first secondary circuit for the time interval [t1, t2].

Following a dead time [t2, t3], the primary switch Q1 is turned on again (with switches Q2, SR1, and SR2 off), such that during time interval [t3, t4] of duration 2, the primary current Ip again builds linearly. At time t4, Q1 is turned off and switch SR2 of the second secondary circuit is turned on, such that the energy in the primary circuit is transferred to the second secondary circuit, leading to a current Is2 (as shown) in the second secondary circuit for the time interval [t4, t5].

Following a dead time [t5, t6], the process is repeated. In this manner, the output ports are energized, with the power allocated to a port proportional to its duration within a whole period. Power transfer from the primary side to the secondary side alternates between output ports.

Critical conduction mode

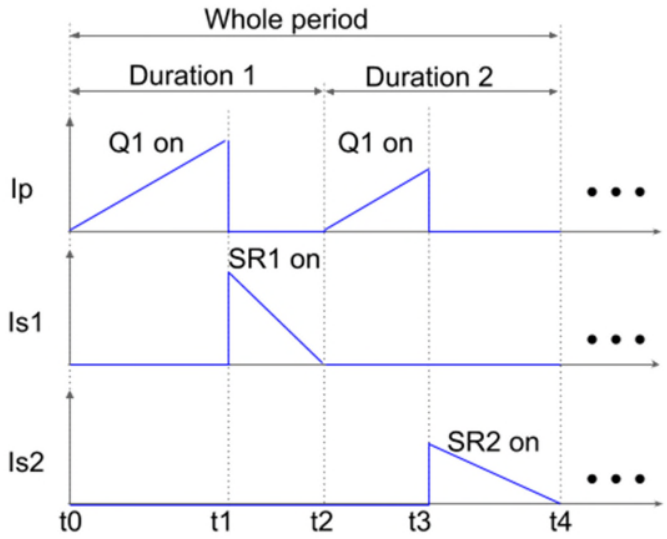

Fig. 4: Control waveforms for critical conduction mode

Fig. 4 illustrates control waveforms for critical conduction mode (CRM), which is a mode that optimizes dead time. Under CRM, the primary circuit current (Ip) and the secondary circuit currents (Is1, Is2) are controlled using their respective switches (Q1, Q2, SR1, SR2) in the manner illustrated in Fig. 4. The waveform pattern, shown in Fig. 4 over a single whole period, is repetitive. A period comprises as many durations (e.g., duration 1, duration 2) as output ports. The ratios of the durations within a whole period determine the power allocations to the output ports. For example, a large duration-1 to duration-2 ratio causes the bulk of the total available power to flow to output port 1.

Within duration 1, during time interval [t0, t1], the primary switch Q1 is on (and its complementary switch Q2 is off), and secondary switches SR1, SR2 are off, such that the primary current Ip builds linearly. At time t1, Q1 is turned off and switch SR1 of the first secondary circuit is turned on, such that the energy in the primary circuit is transferred to the first secondary circuit, leading to a current Is1 (as shown) in the first secondary circuit for a time interval [t1, t2].

At time t2, the primary switch Q1 is turned on again (with switches Q2, SR1, and SR2 off), such that during time interval [t2, t3] of duration 2, the primary current Ip again builds linearly. At time t3, Q1 is turned off and switch SR2 of the second secondary circuit is turned on, such that the energy in the primary circuit is transferred to the second secondary circuit, leading to a current Is2 (as shown) in the second secondary circuit for the time interval [t3, t4].

The waveform pattern within the time interval [t0, t4] is repeated. In this manner, the output ports are energized, with the power allocated to a port proportional to its duration within a whole period. Power transfer from the primary side to the secondary side alternates between output ports.

Combined DCM-CRM mode

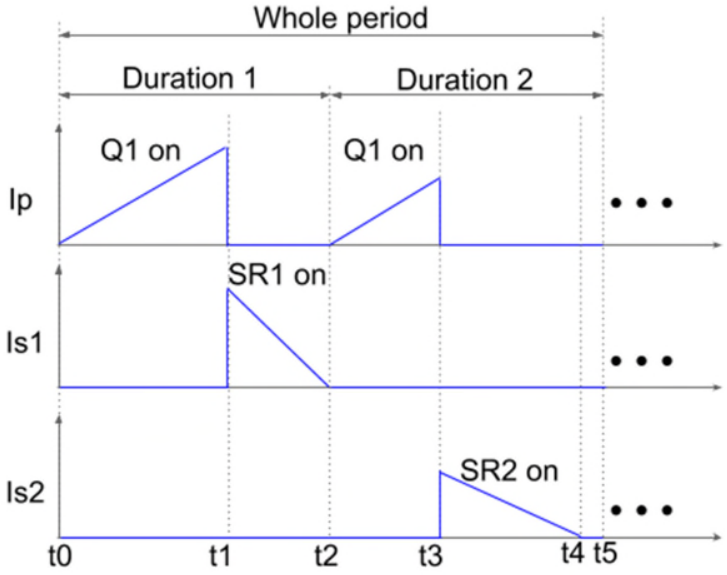

Fig. 5: Control waveforms for combined DCM-CRM mode

Fig. 5 illustrates control waveforms for combined DCM-CRM mode, which is a mode that optimizes dead time and its placement. Under combined DCM-CRM mode, the primary circuit current (Ip) and the secondary circuit currents (Is1, Is2) are controlled using their respective switches (Q1, Q2, SR1, SR2) in the manner illustrated in Fig. 5. The waveform pattern, shown in Fig. 5 over a single whole period, is repetitive. A period comprises as many durations (e.g., duration 1, duration 2) as output ports. The ratios of the durations within a whole period determine the power allocations to the output ports. For example, a large duration-1 to duration-2 ratio causes the bulk of the total available power to flow to output port 1.

Within duration 1, during time interval [t0, t1], the primary switch Q1 is on (and its complementary switch Q2 is off), and secondary switches SR1, SR2 are off, such that the primary current Ip builds linearly. At time t1, Q1 is turned off and switch SR1 of the first secondary circuit is turned on, such that the energy in the primary circuit is transferred to the first

secondary circuit, leading to a current Is1 (as shown) in the first secondary circuit for a time interval [t1, t2].

At time t2, the primary switch Q1 is turned on again (with switches Q2, SR1, and SR2 off), such that during time interval [t2, t3] of duration 2, the primary current Ip again builds linearly. At time t3, Q1 is turned off and switch SR2 of the second secondary circuit is turned on, such that the energy in the primary circuit is transferred to the second secondary circuit, leading to a current Is2 (as shown) in the second secondary circuit for the time interval [t3, t4].

Following a dead time during the interval [t4, t5], the waveform pattern within the time interval [t0, t5] is repeated. In this manner, the output ports are energized, with the power allocated to a port proportional to its duration within a whole period. Power transfer from the primary side to the secondary side alternates between the output ports.

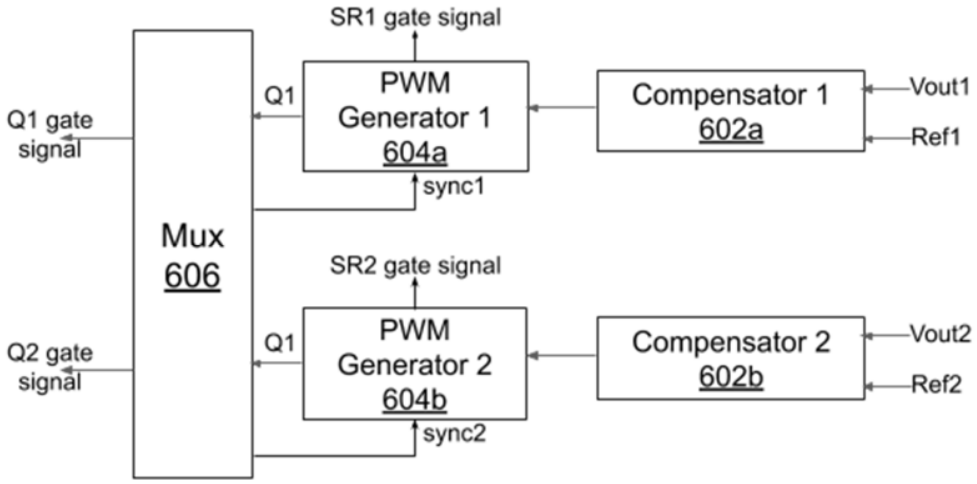

Fig. 6: Control-signal generator circuit

Fig. 6 illustrates an example circuit that generates signals that control the primary-circuit switches (Q1, Q2) and the secondary-circuit switches (SR1, SR2), thereby achieving a target power allocation between output ports. An output port has a target voltage level, denoted Ref1 for port 1, Ref2 for port 2, etc. A compensator, similar to a proportional-integral controller,

samples an output signal, compares it to the corresponding target voltage level, and produces an error signal based on the difference between the two. For example, compensator-1 (602a) produces an error signal based on Vout1 − Ref1 and compensator-2 (602b) produces an error signal based on Vout2 − Ref2.

The error signals are input to pulse wave modulation (PWM) generators that generate gate-control signals for the switches of the corresponding secondary circuits. For example, PWM generator 1 (604a) sets the duty cycle of the square wave that is the gate control signal for SR1 and PWM generator 2 (604b) sets the duty cycle of the square wave that is the gate control signal for SR2. The PWM signals also generate the gate control signals for the primary circuit (Q1, and its complementary signal Q2). A multiplexer (606) generates synchronization signals (sync1, sync2) that activate the PWM generators, and also transmits the gate control signals (Q1, and its complementary signal Q2) to the primary circuit. An example sequence of operations is as follows:

- At the beginning of duration 1, the multiplexer synchronizes PWM generator 1 and passes the Q1 gate signal from PWM generator 1 to Q1. The SR1 gate signal is transmitted from PWM generator 1 to SR1. Duration 1 ends.
- At the beginning of duration 2, the multiplexer synchronizes PWM generator 2 and passes the Q1 gate signal from PWM generator 2 to Q1. The SR2 gate signal is transmitted from PWM generator 2 to SR2. Duration 2 ends.
- The cycle is repeated.

In this manner, the circuit configurations and control techniques described herein achieve single-stage DC-DC conversion with isolated, independent, multi-port output. The converter comprises a coupled inductor with one primary winding, multiple secondary windings each with

a corresponding output port, and a clamping winding. The converter is controlled such that the multiple secondary windings are independent of each other. A power-transfer cycle is divided into several durations, each corresponding to power transfer from the primary winding to an output port. During power transfer to a particular output port, other ports are not impacted. A control circuit is described that generates control signals that achieve a target power allocation between the multiple output ports.

CONCLUSION

This disclosure describes a low cost, low complexity, multi-output charger/adapter that can allocate a total available power smoothly among multiple output ports.