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The Use of Discontiguous Interposers to Stack Multiple Printed Circuit Boards

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The Use of Discontiguous Interposers to Stack Multiple Printed Circuit Boards

Abstract:

This publication describes systems and techniques directed to the use of discontiguous interposers to facilitate the stacking of multiple printed circuit boards (PCBs). In some aspects, an architecture of a subassembly of a system is described that uses the discontiguous interposers to stack multiple PCBs. The architecture is beneficial to heat transfer characteristics while accommodating electromagnetic shielding performance needs of the system. In other aspects, a manufacturing technique is described that panelizes the discontiguous interposers in a fashion that results in manufacturing efficiency gains.

Keywords:

interposer, stacked printed circuit board (PCB), stacked main logic board (MLB), stacked memory module, interposer panelizing, interposer panelization, stacked PCB heat transfer, stacked MLB heat transfer, airflow, air cavity, air gap

Background:

Functionality and performance of features offered through electronic systems continues to evolve through the addition of modules having sensors and/or integrated circuit (IC) components. As an example, smartphones are evolving to include modules having multiple image sensors to improve image-capturing capabilities, radar sensors to enable motion sensing, advanced memory and processor IC components to store and play large media files, and so on.

This increase in modules results in several challenges to the architecture of an electronic system. For example, the increase may negatively impact the form-factor or footprint of the electronic system by necessitating an architecture that includes a large printed circuit board (PCB). Furthermore, and in such an instance, the layout of the large PCB may require electrical trace lengths that compromise performance of the modules in terms of frequency response or bandwidth. To overcome such challenges, architectures of electronic systems are evolving to use subassemblies that include "stacks" of PCBs.

FIG. 1, below, illustrates aspects of an example subassembly of an electronic system that includes a stack of PCBs:

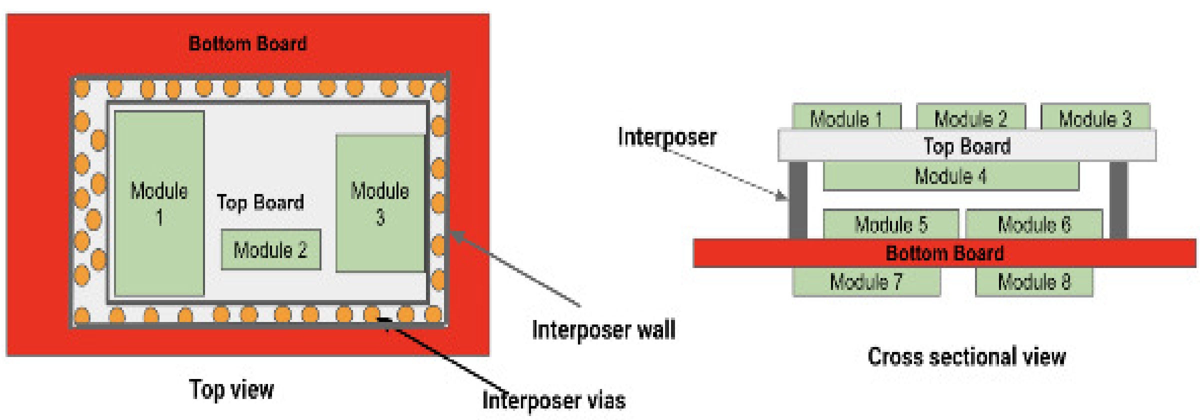

FIG. 1A **FIG. 1B**

The views of FIG. 1A and FIG. 1B illustrate a first PCB (*e.g.*, the top board) that is populated with three modules (*e.g.*, module 1, module 2, module 3) on a surface and populated with another module (*e.g.*, module 4) on an opposing surface. The first PCB, a “double-sided” PCB, may correspond to a main logic board (MLB) populated with a processor module (module 1), two memory modules (modules 2 and 3), and a controller module (module 4).

FIG. 1A and 1B also illustrate a second PCB (*e.g.*, the bottom board) that is populated with additional modules (*e.g.*, the second PCB is also a double-sided PCB). The additional modules (*e.g.*, module 5, module 6, module 7, module 8) may include, for example, an image sensor module, a wireless-communications transceiver module, a video display module, and a radar sensor module.

In general, each of the example PCBs may be a multi-layer PCB fabricated using a glass-reinforced epoxy laminate material such as FR4. Furthermore, and in general, each of the modules may simply be an integrated circuit (IC) component that is surface mounted to the PCB using a solder paste/reflow manufacturing process.

A continguous interposer provides a mechanical structure that creates a standoff and defines a “cavity” between the PCBs. The contiguous interposer may be a continuous interposer. Like the PCBs, the contiguous interposer may also be FR4. The contiguous interposer may electrically connect the PCBs (*e.g.*, for power, signaling, data exchange) using vertical access interconnect (via) traces that are formed through the interposer.

A subassembly of stacked PCBs connected using the continguous interposer has several drawbacks. For instance, manufacturing the contiguous interposer can result in excessive waste of raw material (*e.g.*, FR4). Furthermore, the contiguous interposer may trap heat within the cavity between the PCBs. Such trapped heat can cause degradation in performance of modules within the cavity (*e.g.*, the processor module, the wireless-communications transceiver module), eventually resulting in a thermal shutdown of the electronic system.

Description:

This publication describes systems and techniques directed to the use of discontiguous interposers to facilitate the stacking of multiple printed circuit boards. In some aspects, an architecture of a subassembly of a system is described that uses the discontiguous interposers to stack multiple PCBs. The architecture is beneficial to heat transfer characteristics while accommodating electromagnetic shielding performance needs of the system. In other aspects, a manufacturing technique is described that panelizes the discontiguous interposers in a fashion that results in manufacturing efficiency gains

FIG. 2, below, is a perspective view of an example subassembly, including a stack of PCBs using discontiguous interposers:

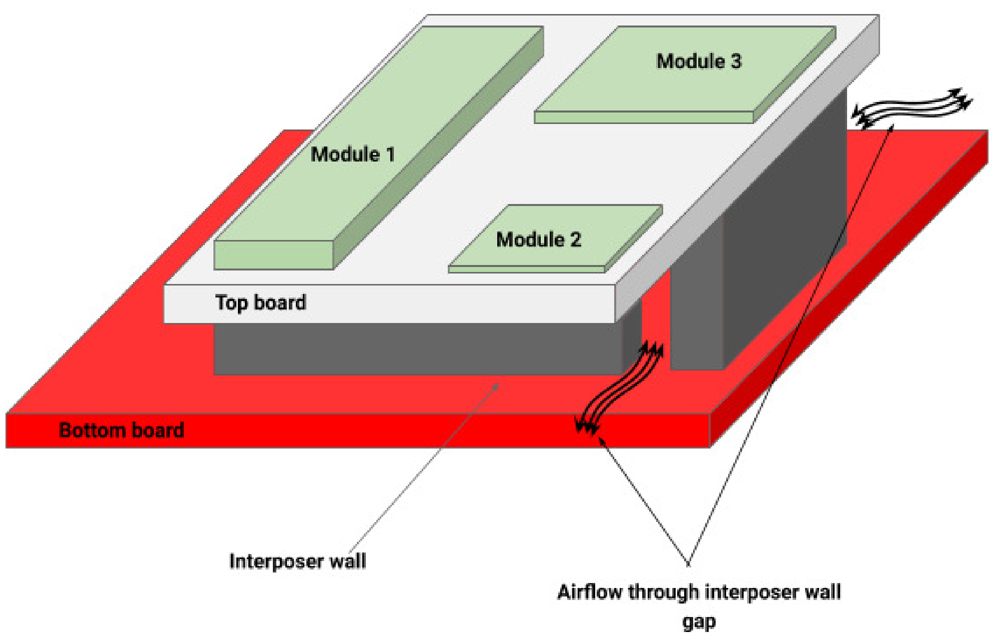

FIG. 2

The discontiguous interposers provide a mechanical structure that defines a cavity between the PCBs. Like the PCBs, the discontiguous interposers may also be FR4. Due to not being formed from a single piece of material (*e.g.*, FR4), the interposers may be arranged as part of the subassembly such that gaps exist between the discontiguous interposers to allow airflow into and out of the cavity. In some instances, the architecture of the subassembly may locate high power modules (or temperature-sensitive modules) near the gaps to maximize heat transfer performance.

FIG. 3, below, illustrates features of example discontiguous interposers in accordance with one or more aspects. The subassembly of FIG. 2 may include the discontiguous interposers of FIG. 3.

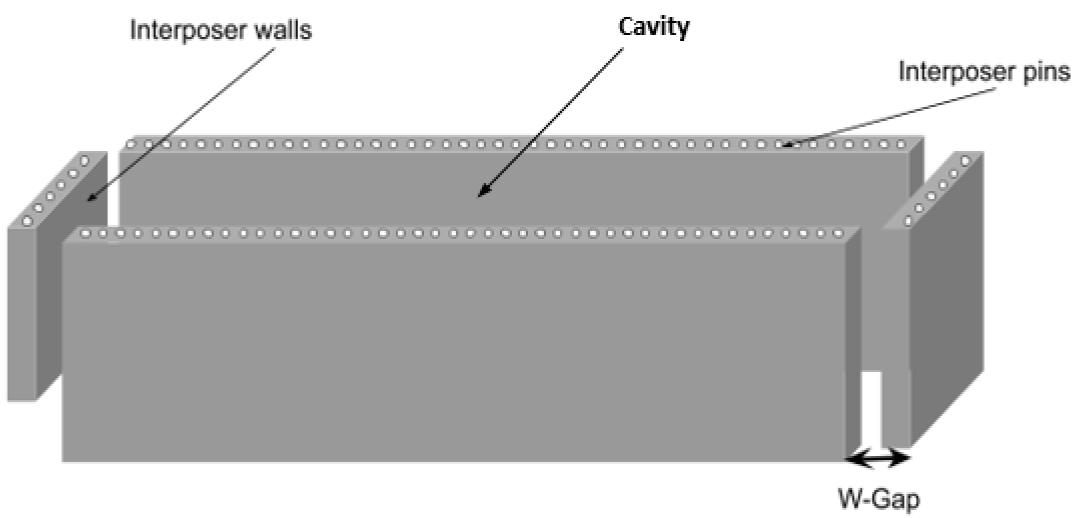

FIG. 3

The discontiguous interposers, in at least some aspects, shield modules in the cavity between the PCBs from electromagnetic interference. Accordingly, and as part of subassembly architecture, widths of the gaps (*e.g.*, "W-gap") may account for targeted circuit operating frequencies. As an example, the width of the gaps may be lesser than a wavelength (λ) of a circuit operating frequency. For instance, and for a circuit operating frequency of 30 Gigahertz (GHz), the widths of the gaps may be < 1 millimeter (mm) to block electromagnetic waves from either entering or escaping the cavity.

Furthermore, and as illustrated in FIG. 3, the discontiguous interposers includes pins that can function as vertical access interconnects (*e.g.*, vias) between the PCBs. In some instances, the pins may be electrically conductive traces that are within layers of the interposer material.

FIG. 4, below, illustrates an example technique for panelizing discontiguous interposers:

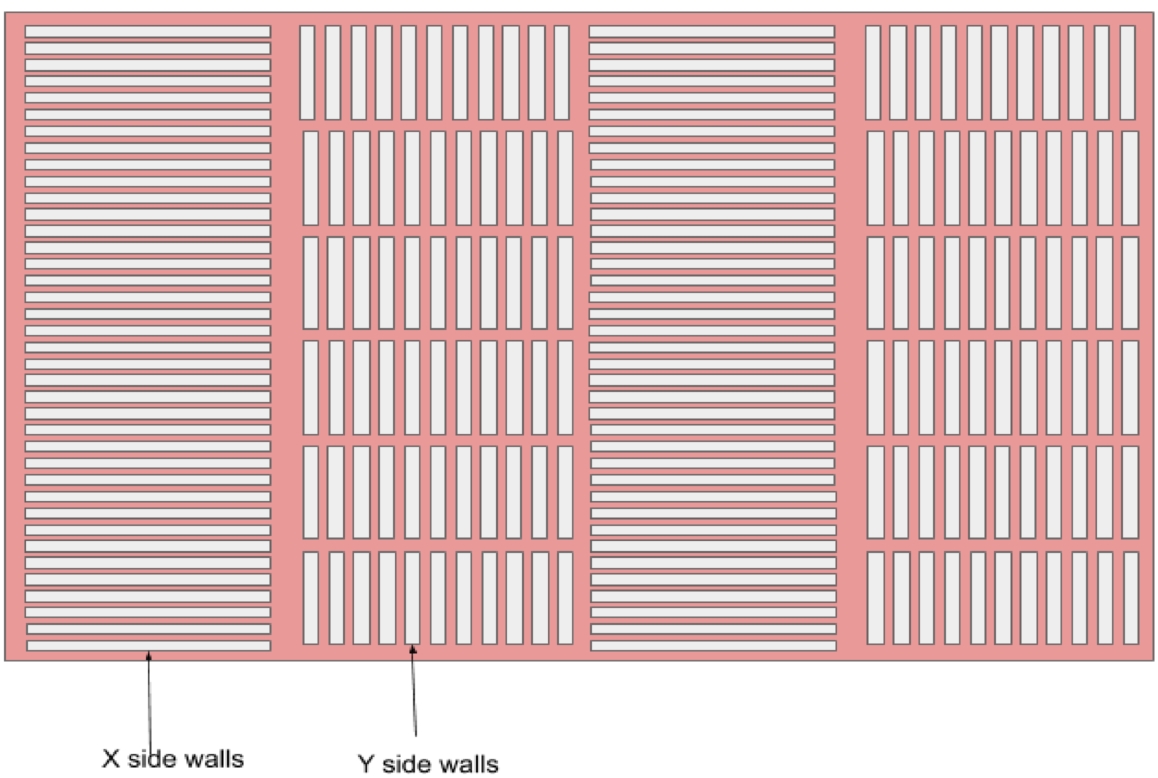

FIG. 4

As illustrated in FIG. 4, the panelizing technique includes using a single panel of a material (*e.g.*, FR4) having a high-density layout of discontiguous interposers. The panelizing technique of FIG. 4 lends itself to gains in manufacturing efficiencies when compared to other panelizing techniques that may be used for contiguous interposers. For example, the high-density layout of the discontiguous interposers, through use of a single panel, can reduce the number of tool setups and/or manufacturing moves that may be required using low-density layouts for contiguous interposers. As a second example, the segmentation/use of multiple, discontiguous interposers in a subassembly reduces waste in panel materials (*e.g.*, a contiguous interposer includes "center" portions of FR4 material that are discarded during manufacturing).

In summary, the described systems and techniques directed to the use of discontiguous interposers to stack multiple printed circuit boards provide multiple benefits. The described systems and techniques are beneficial to heat transfer characteristics while accommodating electromagnetic shielding performance needs. Furthermore, the described system and techniques result in manufacturing efficiency gains.

References:

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