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CONTROL MECHANISM FOR FAST ROLE SWAP

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Control Mechanism for Fast Role Swap

Abstract: A hardware real-time monitor and control circuit shortens the latency of the Fast Role Swap ("FRS") feature of USB power delivery so as to meet the 150us requirement for tSrcFRSwap timing to support faster VBUS slew rates.

This disclosure relates to the field of Universal Serial Bus ("USB") implementations.

A technique is disclosed that shortens the latency of the Fast Role Swap ("FRS") feature so as to meet the 150us requirement for tSrcFRSwap timing to support faster VBUS slew rates.

The Universal Serial Bus Power Delivery Specification R3.0 ("PD3.0") defines a USB Type-C receptacle, plug, and cable which are smaller, thinner, and more robust that prior USB interconnection systems. This allows support of higher power devices via USB.

Fast Role Swap is an optional feature of the PD3.0 specification. A challenge exists where VBUS slew rate limits do not apply, and thus the VBUS may transition faster than specified. The latency of the Fast Role Swap ("FRS") feature includes the VBUS drop detection delay time of the PD controller, the GPIO sending a signal to pull up the enable pin of the 5V load switch, and the VBUS being raised to 5V from lower voltage. In many cases it is difficult to meet the 150us requirement for tSrcFRSwap with this implementation.

According to the present disclosure, and as understood with reference to the Figure, a hardware real-time monitor and control circuit 10 shortens the latency of FRS to meet the tSrcFRSwap 150us requirement.

Instead of VBUS detection for fast slew rates being handled by the power delivery ("PD") controller, the hardware real-time monitor circuit detects the fast slew rate of VBUS drop condition. The Reverse Current Protection ("RCP") IC behaves as an ideal diode on the 5V rail, causing FET turn on immediately if an RCP event occurs. Recovery from an RCP event is automatic.

The monitor circuit detection voltage level is in the range of about 5.5V to about 6V. When VBUS raises above 6V, the additional control signal 20 will pull up enable pin 30 of the RCP IC. When VBUS quickly drops below 6V, the additional control signal 20 of the real-time monitor and control circuit 10 pulls the enable pin 30 of the RCP IC low. A controllable delay time for pulling the enable pin low is defined by R1 40 and C1 50.

The PD controller can still drive the enable pin 30 of the RCP IC via the PD controller signal 25 for slower VBUS slew rates, and thus the hardware real-time monitor and control circuit 10 does not violate the original PD controller operation or 5V output behavior.

The disclosed technique of a real time monitor circuit with controllable delay allows the VBUS to drop quickly based on device loading at the FRS condition, and meet the tSrcFRSwap 150us requirement.

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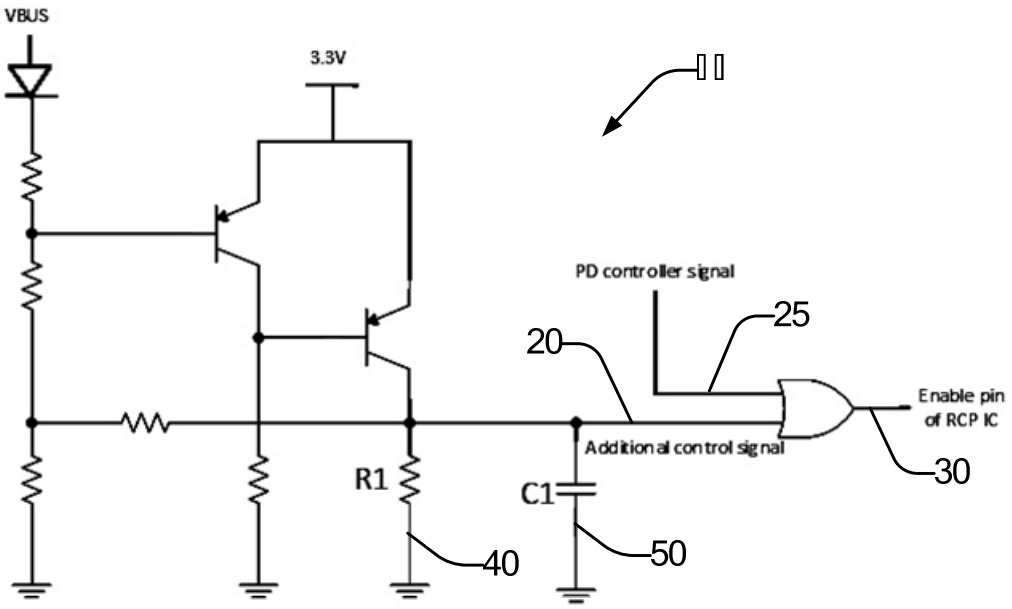
VBUS
3.3V
PD controller signal
25
20
Enable pin
of RCP IC
Additional control signal
30
R1
C1
40
50