August 19, 2019

High-density voltage regulator using multi-fed polygon inductor

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ABSTRACT

Data centers today employ powerful CPUs and GPUs that consume a significant amount of current, e.g., up to a thousand amperes of current. To mitigate large thermal losses in the power delivery network that occur at such high amperages, voltage regulators (VR) are moved closer to their loads, e.g., vertically below the loads. For a VR to fit in the tight space below the load, it must be of high density and integrate the decoupling capacitors that often occupy the space below the load. This disclosure describes a scalable, multi-fed-polygon (MFP) coupled inductor that is optimized for vertical power delivery. The polygon shape of the inductor enables it to interface with power stage components in several directions, resulting in high utilization of magnetic core flux density, reduced physical dimensions, and flexible layout possibilities. Decoupling capacitors are fit below the MFP inductor, resulting in further space saving and excellent transient response.

KEYWORDS

- Power delivery network
- Multi-fed inductor
- Polygon inductor
- Vertical power delivery
- Decoupling capacitor
- High density VR
- Voltage regulator

BACKGROUND

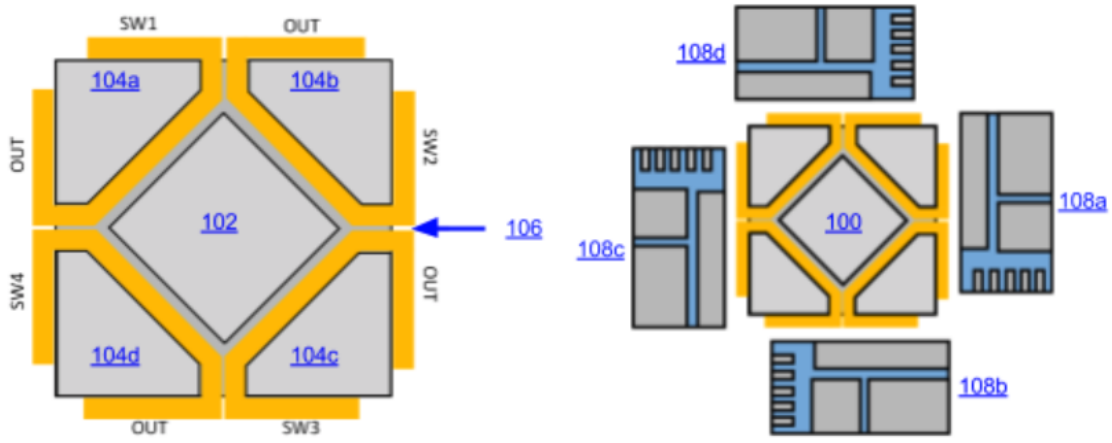
Data centers today employ powerful CPUs and GPUs that consume a significant amount of current, e.g., up to a thousand amperes of current. Traditional power delivery techniques place the point of load voltage regulator (PoL VR) on the side of the processor unit such that power is delivered laterally to the processor. However, at the high amperages of modern ASICs, the distance from the VR to its load (the processor) causes a high voltage loss (IR drop) across the power delivery network which may be unacceptable in some situations. The load not only suffers from low voltage, the IR drop causes other undesirable effects, e.g., thermal loss, high temperature, lower reliability, poor dynamic voltage regulation, etc.

To mitigate large thermal losses in the power delivery network that occur at such high amperages, voltage regulators (VR) are moved closer to their loads, e.g., vertically below the loads. For example, a voltage regulator can be vertically mounted either on the bottom side of the motherboard or on the bottom of the processor package substrate. By doing so, power delivery from VR to the processor is on a shorter path with reduced impedance. Such vertical power delivery techniques not only reduce thermal losses, they also deliver subsidiary benefits, e.g., better transient response, lower complexity, higher reliability, greater design flexibility, better manufacturing yield, etc. For a voltage regulator to fit in the tight space vertically below its load, it must be of high density, and it must also integrate the decoupling capacitors that often occupy the space below the load.

DESCRIPTION

This disclosure describes a scalable, multi-fed-polygon (MFP) coupled inductor that is optimized for vertical power delivery. The polygon shape of the inductor enables it to interface with power stage components in several directions, resulting in high utilization of magnetic core

flux density, reduced physical dimensions (reductions of up to 70% of the size of conventional inductors), and flexible layout possibilities. Decoupling capacitors, e.g., of multi-layer ceramic type, are fit below the MFP inductor, resulting in further space saving and excellent transient response.



(A) (B)

Fig. 1: An *N*=4 phase MFP coupled inductor: (A) Cross-section; (B) MFP coupled inductor in relation to its power stages

Fig. 1A illustrates a cross-sectional view of a 4-phase MFP coupled inductor, per techniques of this disclosure. The inductor in this example has *N=4* small posts (104a-d) and one big post (102). The *N* small posts generate magnetizing flux for open-loop self-inductance for each of *N* phases, and the one big post provides a common mode leakage flux path that generates the common mode output inductance. A copper coil (106) is wound around each of the posts. There are as many phases as there are small posts, and each phase has a pulse-width modulated (PWM) waveform applied at locations SW1 through SW*N*. The PWM waveforms are offset in phase from each other. The output voltage of the inductor is delivered on the terminals marked OUT. The power stages and the MFP coupled inductor together comprise a power delivery module.

Fig. 1B illustrates the MFP coupled inductor (100) situated in relationship to its power stages (108a-d), e.g., as laid out on a module PCB. The power stages comprise voltage regulator components such as field-effect transistors (FETs) and are placed on each side of the inductor polygon to feed power into it. For ease of manufacturing, the MFP coupled inductor features a symmetric mechanical structure with optimized dimension aspect ratios for each post. For example, a 10mm x 10mm 4-phase design delivers as much as a maximum 400 Amperes and a thermal design current of as much as 160 Amperes, while occupying a volume that is 70% lower than a conventional inductor.

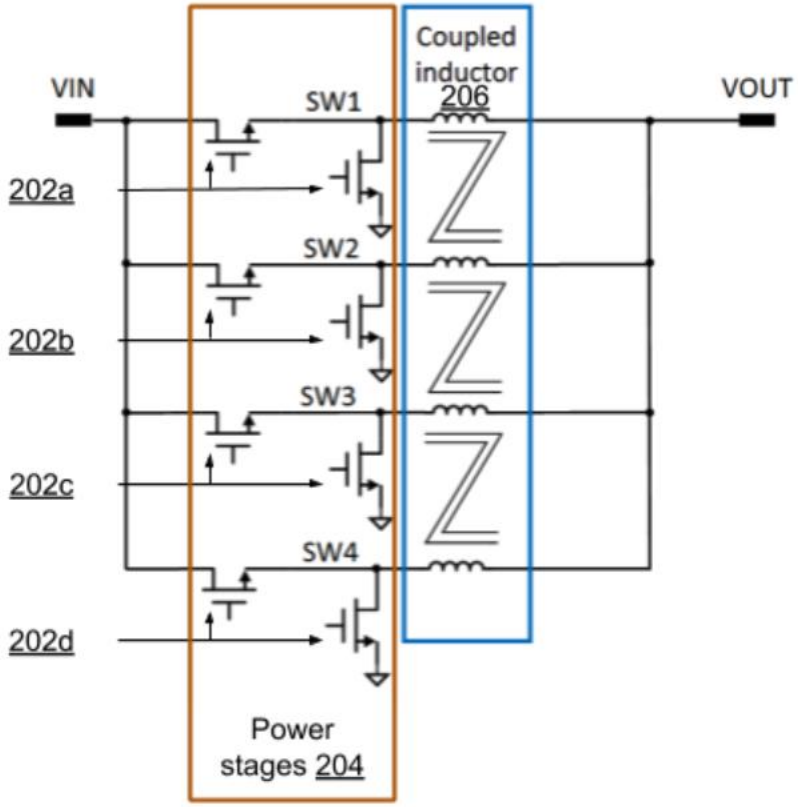


Fig. 2: Circuit equivalent of a buck voltage regulator using an *N*=4 phase MFP coupled inductor

Fig. 2 illustrates the circuit equivalent of a buck voltage regulator using an *N*=4 phase MFP coupled inductor, e.g., the inductor of Fig. 1A. The power stages (204) that ring the inductor comprise *N* pairs of field-effect transistors (202a-d). The input voltage VIN is applied to

a terminal of each of the FET pairs. The source-drain interconnect (SW1 through SW*N*) of an FET pair is connected to the corresponding lead of the coupled inductor (206). The coupled inductor is formed out of the *N* small posts, one big post, and the copper windings around the posts. The output voltage VOUT is obtained at the inter-connected output leads of the coupled inductor.

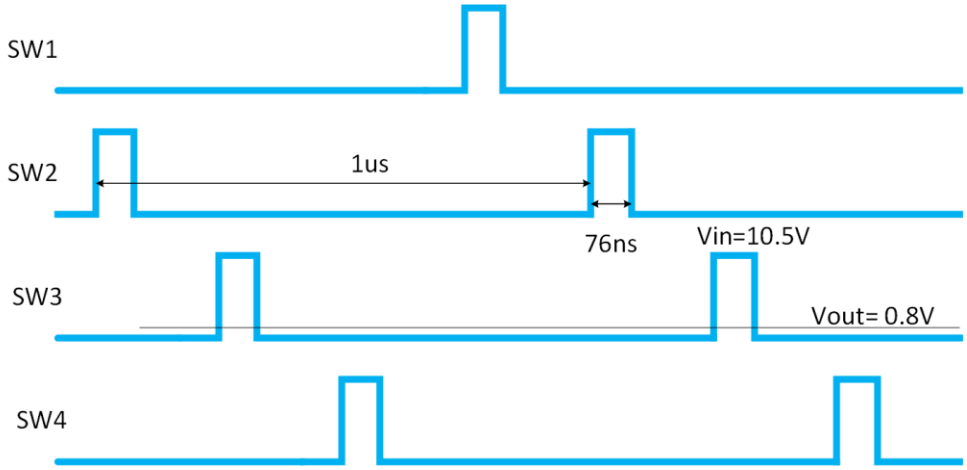


Fig. 3: PWM waveforms applied at the source-drain interconnects of the power stages

Fig. 3 illustrates pulse-width modulated (PWM) waveforms applied at the source-drain interconnects (SW1 through SW*N*) of the FET pairs of the power stages. As shown, the PWM waveforms are interleaved with each other, e.g., offset in phase from each other. The PWM waveforms drive the MFP coupled inductors in order to generate magnetic flux. Shown are representative values for the pulse-width and period of the PWM waveforms, and for the input and output voltages of the power delivery module.

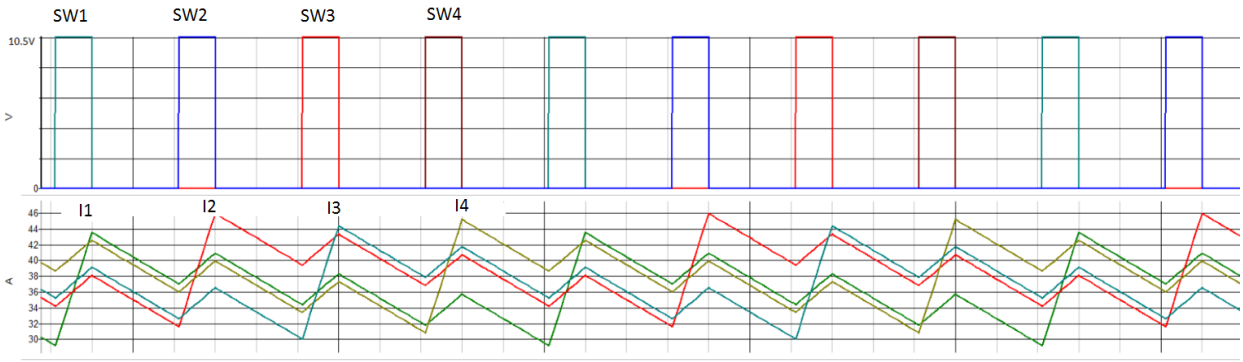
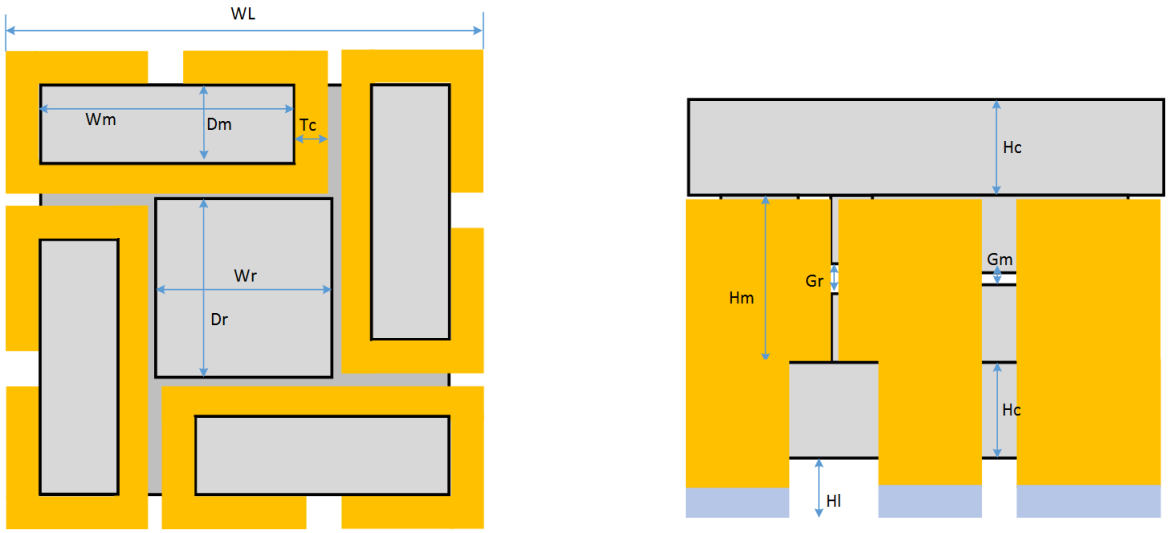


Fig. 4: Output current in relation to the driving PWM voltage waveforms

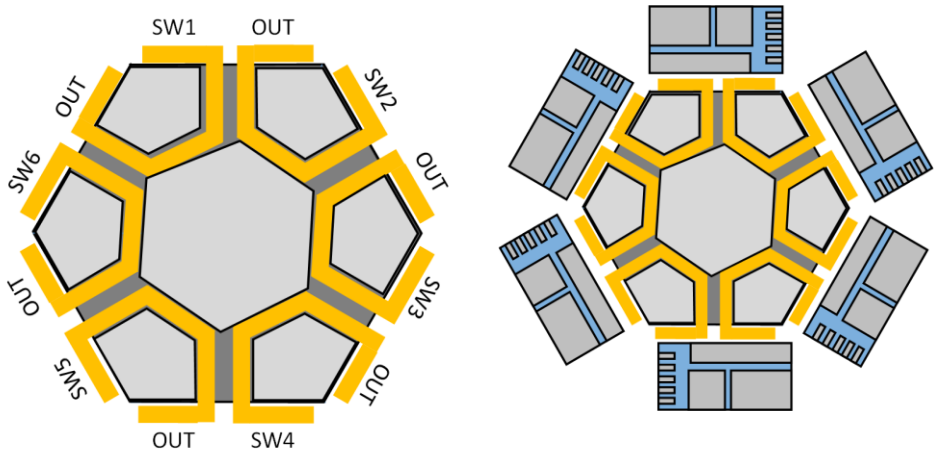
Fig. 4 illustrates output current (*I1* through *I4*) in relationship to the driving PWM voltage waveforms in an *N*=4 phase power delivery module. As is seen, the ripple in the current waveforms as a fraction of their amplitudes is relatively low. Also, the current fed to the load is the sum *I1+I2+I3+I4* of the per-phase currents; this sum has even lower ripple than its constituents.



(A) (B)

Fig. 5: (A) cross-section; and (B) Side view of an *N*=4 phase MFP coupled inductor

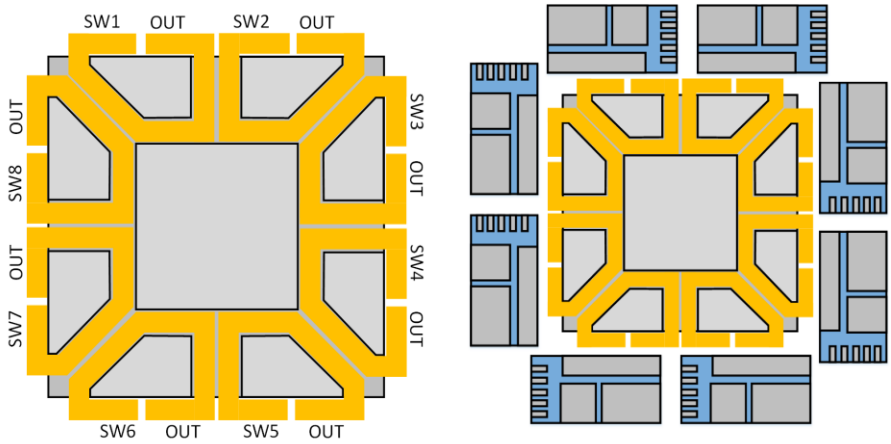
Fig. 5 illustrates an alternate *N*=4 phase MFP coupled inductor structure in cross-sectional (Fig. 5A) and side (Fig. 5B) views.



(A) (B)

Fig. 6: An *N*=6 phase MFP coupled inductor: (A) cross-section; (B) in relation to its power stages

Fig. 6 illustrates an *N*=6 phase MFP coupled inductor, per techniques of this disclosure. Fig. 6A illustrates a cross-sectional view of the *N*=6 phase MFP coupled inductor and Fig. 6B illustrates the inductor in relation to its power stages, e.g., as laid out on a module PCB.



(A) (B)

Fig. 7: An *N*=8 phase MFP coupled inductor: (A) cross-section; (B) in relation to its power stages

Fig. 7 illustrates an *N*=8 phase MFP coupled inductor, per techniques of this disclosure. Fig. 7A illustrates a cross-sectional view of the *N*=8 phase MFP coupled inductor and Fig. 7B illustrates the inductor in relation to its power stages, e.g., as laid out on a module PCB.

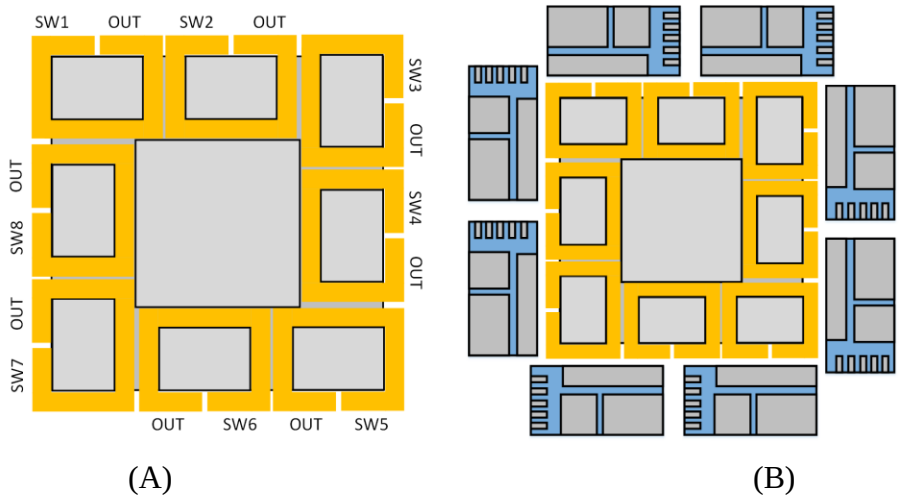


Fig. 8: An *N*=8 phase MFP coupled inductor: (A) cross-section; (B) in relation to its power stages

Fig. 8 illustrates an alternate implementation of an *N*=8 phase MFP coupled inductor, per techniques of this disclosure. Fig. 8A illustrates a cross-sectional view of the *N*=8 phase MFP coupled inductor and Fig. 8B illustrates the inductor in relation to its power stages, e.g., as laid out on a module PCB.

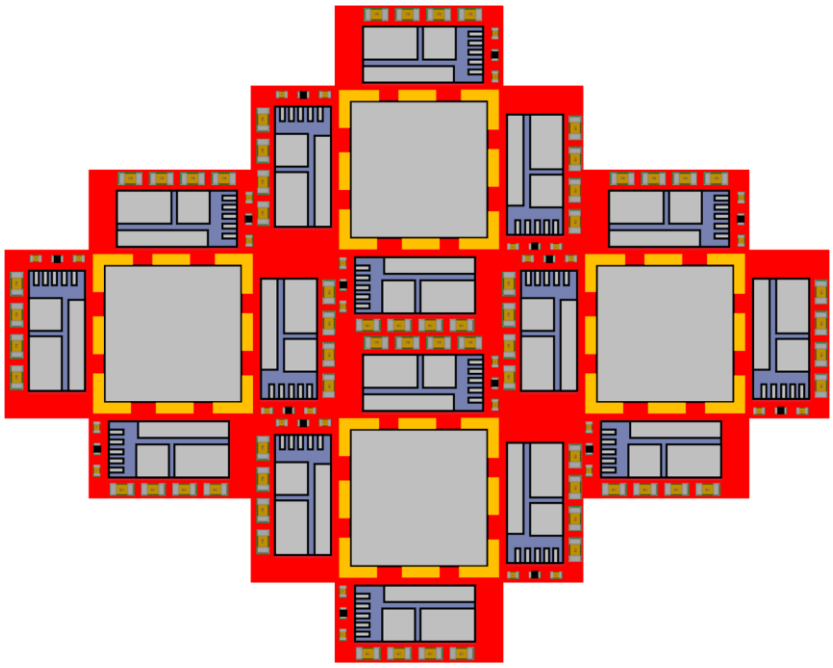


Fig. 9: An example layout on a module PCB of four power delivery modules each based on an *N*=4 phase MFP coupled inductors

Fig. 9 illustrates a top view of an example high-density layout on a module PCB of four N=4 phase MFP coupled inductors and their associated power stages. The total number of phases achieved by this layout is sixteen.

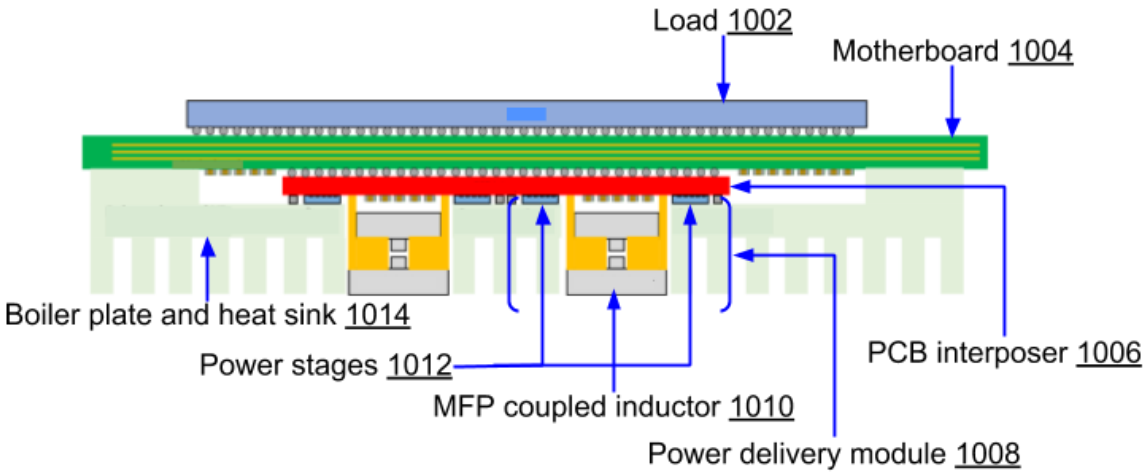


Fig. 10: Side view of vertical power delivery in operation

Fig. 10 illustrates a side view of vertical power delivery in operation, e.g., connected vertically underneath a load. The load (1002), e.g., an ASIC, GPU, CPU, etc., is seated on a motherboard (1004) using an appropriate surface-mount technology, e.g., ball-grid array, land-grid array, etc. Two power delivery modules are shown, each connected to the motherboard via a PCB interposer (1006) and situated vertically below the load. A power delivery module (1008) comprises a high-density MFP coupled inductor (1010) and power stages (1012), as explained before. A boiler plate and heat sink (1014) absorbs heat generated by the power delivery module and by the load.

In this manner, the techniques of this disclosure enable high-density, highly integrated voltage regulation optimized for high-current vertical power delivery. The MFP coupled inductor described herein fits easily into the small region at the bottom of a motherboard under the load, e.g., CPU, GPU or other processor, and enables high-efficiency vertical power delivery.

Decoupling capacitors that earlier occupied the region below the load are fit below the MFP inductor, further reducing the overall space occupied by the power delivery module and improving transient power response.

CONCLUSION

This disclosure describes a scalable, multi-fed-polygon (MFP) coupled inductor that is optimized for vertical power delivery. The polygon shape of the inductor enables it to interface with power stage components in several directions, resulting in high utilization of magnetic core flux density, reduced physical dimensions, and flexible layout possibilities. Decoupling capacitors are fit below the MFP inductor, resulting in further space saving and excellent transient response.