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DUAL LAYOUT FOR SUPPORTING X16 AND X32 VRAM ON THE SAME PCB BOARD

HP INC

Dual layout for supporting X16 and X32 VRAM on the same PCB board

This disclosure related to place VRAMs back-to-back on TOP and Bottom sides to support two different VRAM SKUs.

A PCB co-layout design is disclosed that by BOM options to Install VRAMs on one side only to support x32 SKU's or install VRAMs on both TOP and Bottom sides to support X16 SKUs.

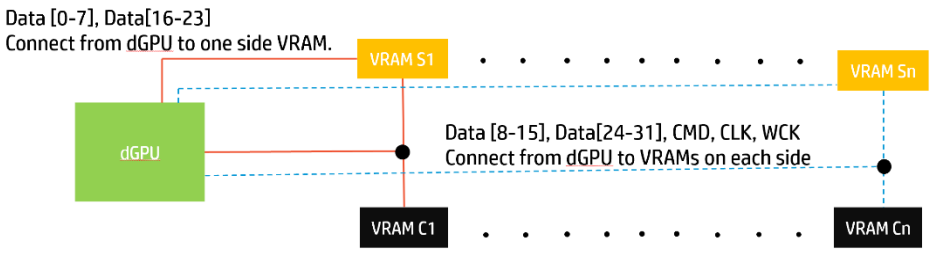
The unique design here is that we are implementing 2GB and 4GB options with 64-bit VRAM interface using either x32 or x16 parts. Therefore, the routing challenge is different than supporting 2GB and 4GB with 64-bit and 128-bit interface respectively.

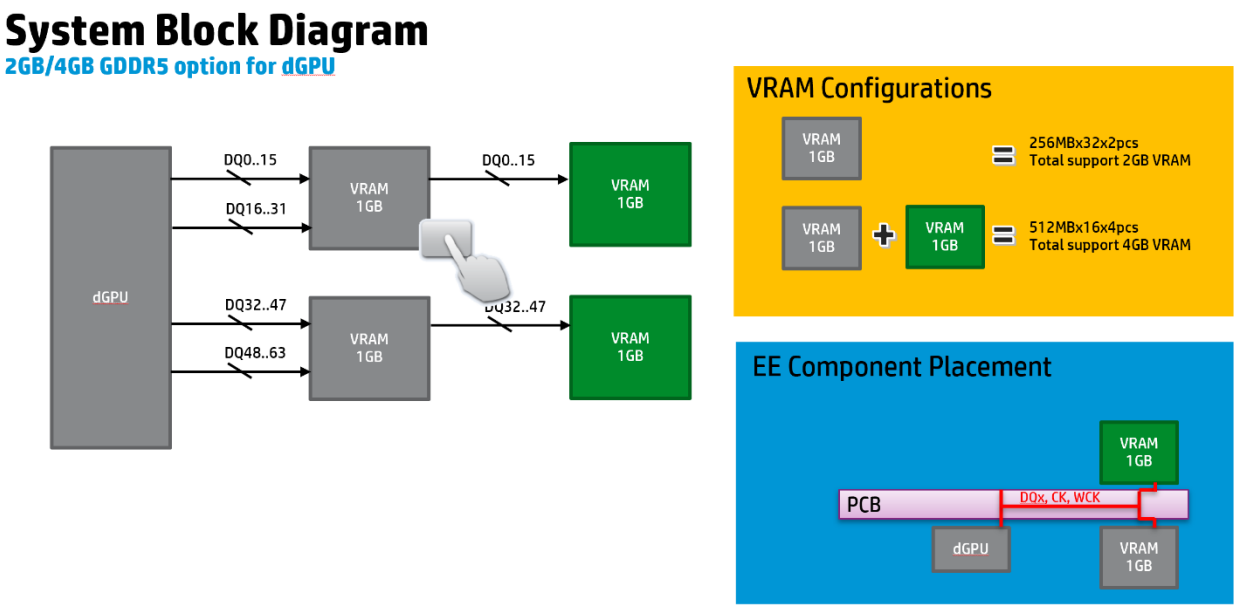
To date layout design to support two different dGPU memory frame buffers, we have to design two different PCBs, one for x16 VRAMs, the other for x32 VRAMs. Biggest challenge is we couldn't support 2GB and 4GB sku due to memory density using same memory foot print. Either we will have to make 2GB PCB sku or 4GB PCB sku. Also, GPU can only support 64-bit memory interface. But when I looked at memory pin-out for x16 vs x32 they were using same package and pin-out.

We figure out a way to support board layout that allows these options on same PCB with no stub and zero ohm resistors. Support different video memory size (for e.g. 2GB and 4GB), and different memory bus width (for e.g. 64-bit and 128-bit) with new memory density 8G-bit (to address EOL of 4G-bit current memory Capacity) on common PCB.

Different memory frame buffer with different memory density, we have a lot of VRAM SKUs to support different VRAM capacity. Additionally, we have 64/128/192/256 bits dGPU in the market. This solution can help to reduce dGPU/VRAM complexity to share the same PCB board. With this Co-layout design, we can help to reduce PCB/PCBA SKUs, use BOM option to control different VRAM SKUs. It also helps reduce validation resource since the PCB board is leveraged between X16 and X32. Additionally, we can get the benefit for cost saving and maintaining two different PCBs and debug resource.

PCB Layout concept,





Disclosed by Yi Ko Hsiao, Rahul V Lakdawala and Richard Lin, HP Inc.