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Frequency division multiple supply (FDMS) for fast-response power delivery

ABSTRACT

Traditional power delivery networks (PDN) to ASICs have a bandwidth that extends to about 100 kHz such that these PDNs respond with adequate speed and meet performance specifications if the transient load current changes at a rate slower than 100 kHz. As ASICs become more computationally powerful, not only does their current consumption go up, their current transients undergo relatively rapid slew, e.g., with a bandwidth exceeding 10 MHz. The bandwidth mismatch between the PDN and the current demand of the ASIC causes a substantial loss in efficiency.

This disclosure describes a PDN comprising an ensemble of three or more power supplies optimized to differing frequency ranges. A power supply from the ensemble automatically kicks in when transient currents arise with a bandwidth that includes the frequency range of the power supply. Power is delivered across the entire ASIC bandwidth at optimal efficiency and with excellent transient response.

KEYWORDS

- Frequency division multiple supply
- FDM power supply
- Power delivery network (PDN)
- PDN bandwidth
- Transient current
- PDN impedance
- ASIC

BACKGROUND

Traditional power delivery networks to application-specific integrated circuits (ASICs) or other loads, e.g., CPUs, GPUs, etc., include a passive power delivery network (PDN) and a voltage regulator (VR) that sits next to the ASIC on the motherboard. The PDN couples the voltage regulator to the chip die of the load. The voltage rails of the load ASIC are to meet certain criteria in terms of voltage noise across the entire frequency spectrum in order to achieve design performance. Electrically, the output impedance of the PDN as seen from the point of load, e.g., the chip die, must be maintained below a target impedance in order to control voltage noise within budget under worst-case transient loads.

The voltage regulator can typically respond to transient load currents from DC up to a certain frequency, called the VR bandwidth. The VR bandwidth is typically 100 kHz, e.g., the VR can respond adequately to load transients between DC and 100 kHz. Above the VR bandwidth, the response is dependent on the frequency characteristics of the PDN. The PDN being a low-pass, complex-impedance network that includes decoupling capacitors, parasitic inductances, ESRs, etc., transient current loads beyond the regulator bandwidth result in poor power-conversion efficiency. Designing voltage regulators with higher bandwidth can alleviate the low bandwidth of the PDN to some extent, but again, it comes at a cost of power-conversion efficiency at increased switching frequency.

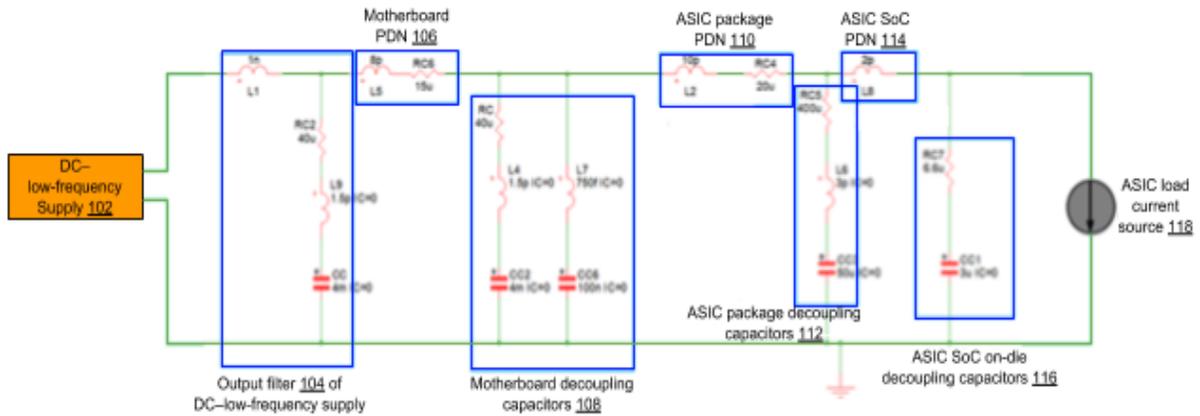


Fig. 1: Power delivery network with traditional voltage regulator

Fig. 1 illustrates a power delivery network with a traditional voltage regulator. The traditional voltage regulator, as explained above, can respond adequately to transients only up to a certain bandwidth; hence it is referred to as a DC-low-frequency power supply (102). The DC-low-frequency power supply delivers power to an ASIC load, represented in Fig. 1 as a current source (118). Between the power supply and the load is a power delivery network, which comprises an output filter (104) of the DC-low-frequency power supply; a motherboard PDN (106); motherboard decoupling capacitors (108); an ASIC package PDN (110); ASIC package decoupling capacitors (112); ASIC System-on-a-Chip (SoC) PDN (114); ASIC SoC on-die decoupling capacitors (116); etc.

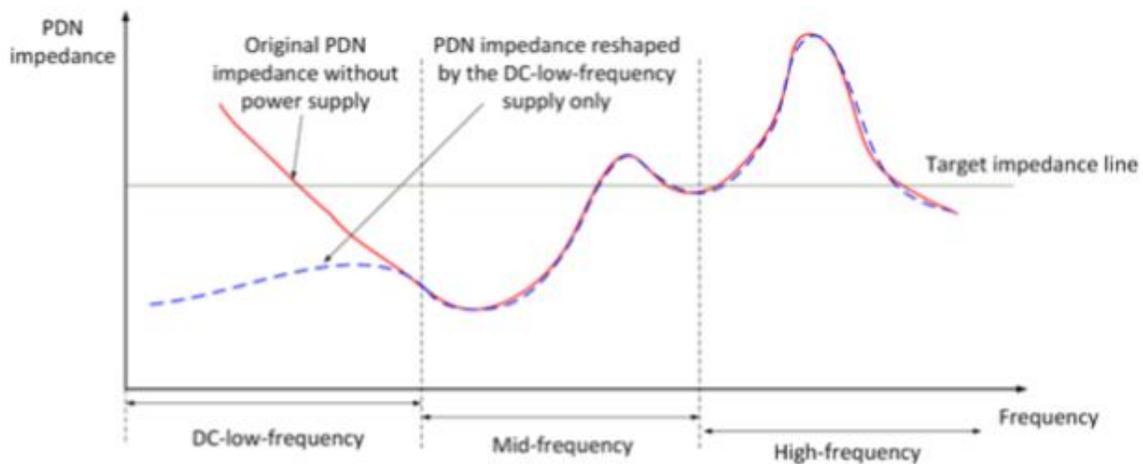


Fig. 2: Frequency response of traditional PDN

Fig. 2 illustrates a typical frequency response of a traditional power delivery network as seen from the load, e.g., the ASIC chip die. The X-axis is divided into three example ranges, e.g., DC–low-frequency (0-100 kHz); mid-frequency (100 kHz-10 MHz); and high frequency (> 10 MHz). The red curve is the impedance of the passive parts of the power delivery network, e.g., when the DC–low-frequency power supply is disconnected. Ideally, the frequency response is below the target impedance line for all frequency ranges. However, it is seen in the red curve that there are at least two resonant peaks that exceed the target impedance, one in the mid-frequency band and the other in the high-frequency band. The mid-frequency resonant peak is usually caused by the resonance between ASIC package capacitors and PCB board vias-package pin inductances. The high frequency resonant peak is usually caused by the resonance between package vias-bumps inductances and on-die decoupling capacitors.

When a carefully designed DC–low-frequency power supply is connected to the passive PDN, the dotted-blue impedance curve results. The dotted-blue impedance curve, the combined impedance of the power supply and the passive PDN, does meet the target impedance specification at low frequencies. As a result, the voltage noise seen by the ASIC die has relatively small low-frequency ripple and DC error under most load conditions. However, the dotted-blue impedance curve fails to meet the target impedance specification at the mid- and high-frequency ranges. Under the dotted-blue impedance response, power delivery to high-performance ASICs, with their high current demands and wide transient current bandwidths, becomes inefficient. Also, it is difficult to design the passive PDN impedance to be below the target impedance across the entire spectrum.

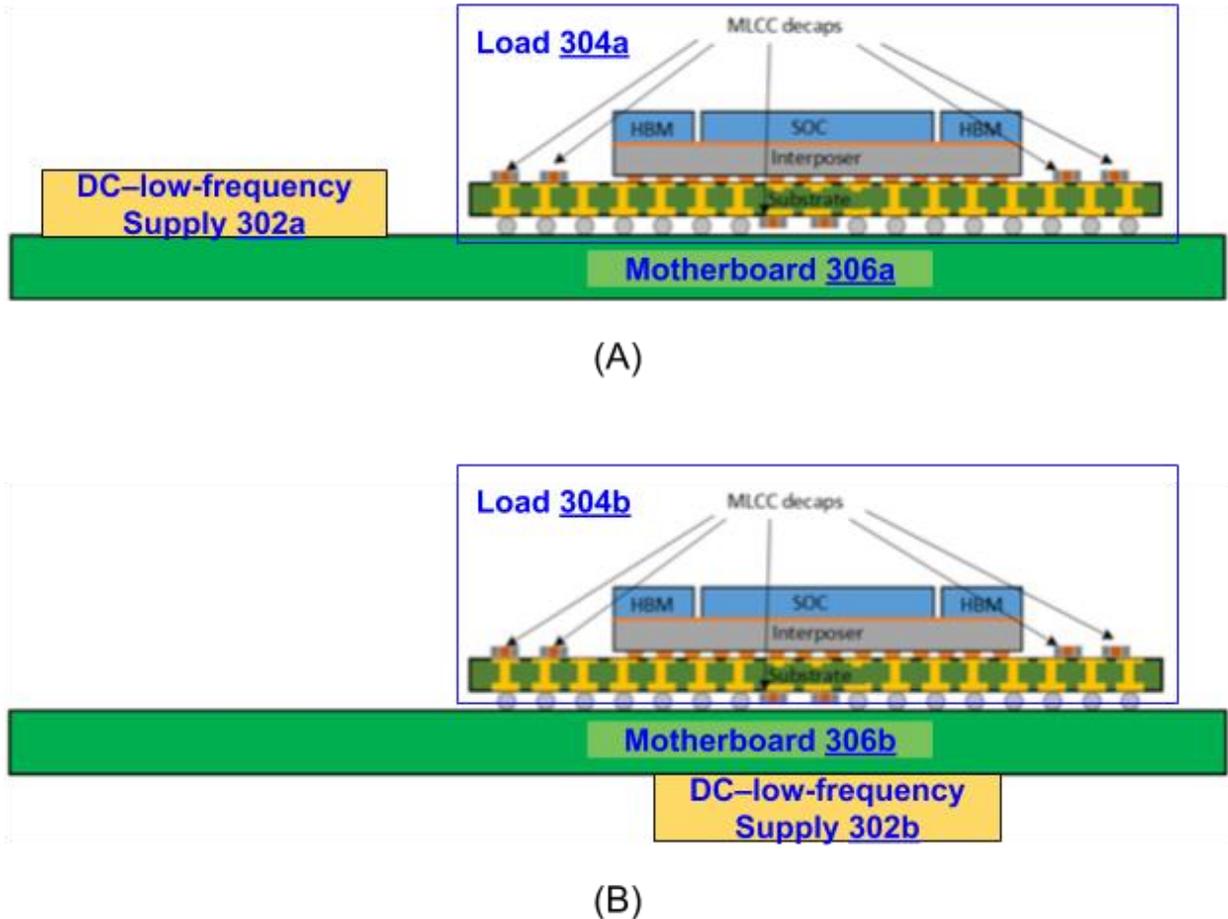


Fig. 3: Types of layouts of DC-low-frequency power supply in relation to load: (a) Lateral power delivery; (b) Vertical power delivery

Fig. 3 illustrates two physical layouts of a power delivery network. In Fig. 3A, lateral power delivery, the DC-low-frequency power supply (302a) is located next to the load (304a) on a motherboard (306a). In this context, the load includes the ASIC, e.g., SoC, and associated components such as high-bandwidth memory, interposer, substrate, multi-layer ceramic decoupling capacitors, etc. In Fig. 3B, the DC-low-frequency power supply (302b) is located underneath the load (304b) on the opposite side of the motherboard (306b). Although the layout of Fig. 3B is effective in improving the low frequency response of the power supply, both layouts have poor mid- and high-frequency responses.

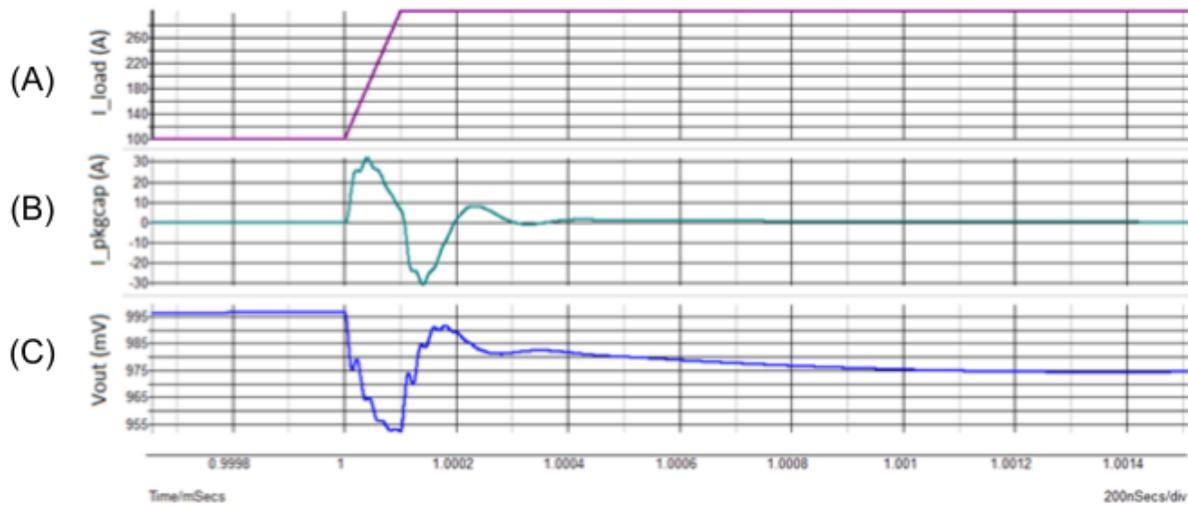


Fig. 4: Time-domain transient responses of a traditional DC–low-frequency power supply: (A) A step jump in load current demand; (B) Response as measured by package capacitor current; (C) Response as measured by power supply output voltage

Fig. 4 further illustrates the poor mid- and high-frequency transient responses of a traditional DC–low-frequency power supply. A step jump in current demanded by the load occurs (Fig. 4A). The package decoupling capacitors engage to discharge and supply current to the load (Fig. 4B). The output voltage of the power supply (Fig. 4C) experiences not only unacceptably high oscillations but also a voltage droop, e.g., a transient trend towards low voltage after the current step has occurred. This voltage droop is dictated by the mid-to-high frequency impedance response of the PDN network. Due to the limited decoupling capacitor density that can be integrated within the processor package, this voltage droop is further exacerbated. For example, the voltage level can exceed the specified AC noise level such that the load processor is forced to run at a higher voltage set-point with higher power consumption, even when in normal operation.

DESCRIPTION

This disclosure describes a PDN that comprises an ensemble of three or more power supplies, each optimized to differing frequency ranges. A power supply from the ensemble automatically kicks in when transient currents arise with a bandwidth that includes the frequency range of the power supply. Power is delivered across the entire ASIC bandwidth at an optimal efficiency.

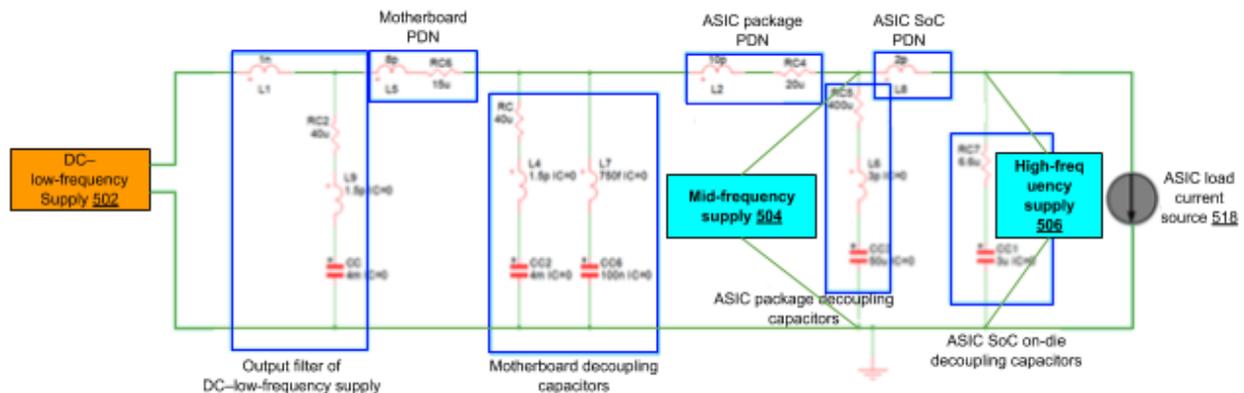


Fig. 5: Power delivery network employing frequency-division multiple supply

As illustrated in Fig. 5, in addition to the DC-low-frequency power supply (502) that supplies a load (518), other power supplies in parallel to the DC-low-frequency power supply, e.g., a mid-frequency supply (504) and/or a high-frequency power supply (506), also supply the load. As illustrated, the three power supplies are at different physical locations in the power delivery network. For example, the mid-frequency supply is incorporated at the processor package level to effectively enhance the on-package decoupling capacitance. The high-frequency supply is incorporated at the processor chip die level to effectively enhance the on-die decoupling capacitance. Both the mid- and high-frequency supplies operate in a manner similar to decoupling capacitors that shape the mid- and high-frequency PDN impedance. Because each

power supply is optimized to a different frequency range, the techniques are referred to as “frequency-division-multiple-supply,” or FDMS.

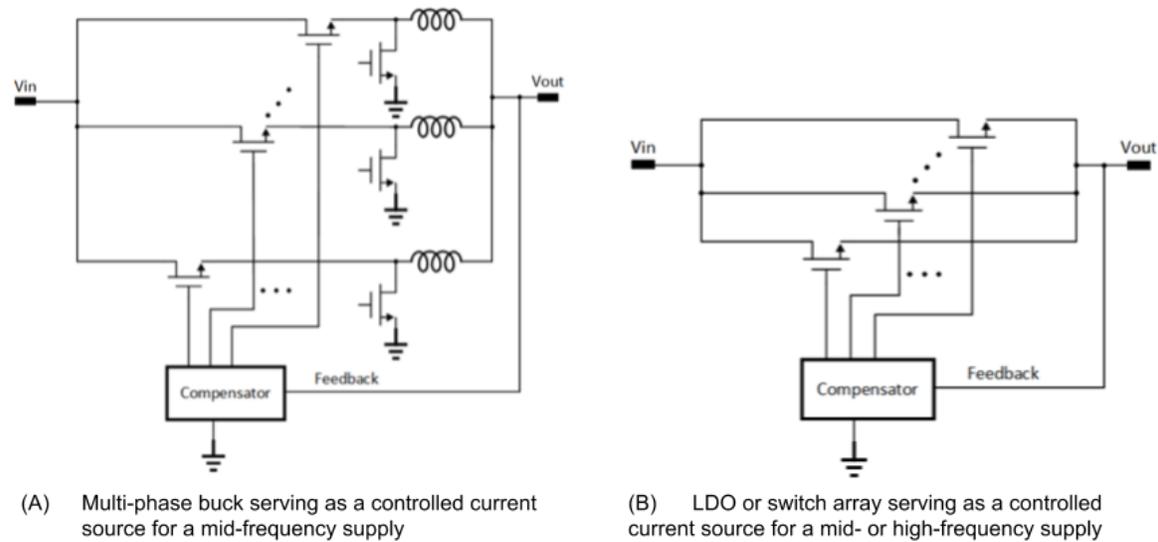


Fig. 6: Circuit topologies for mid-frequency and high-frequency power supplies.

Fig. 6 illustrates circuit topologies for the mid-frequency and high-frequency power supplies. The mid-frequency supply can be constructed from multi-phase buck voltage regulators switching, e.g., at tens of MHz (Fig. 6A), or a low-dropout (LDO) voltage regulator (Fig. 6B). In both cases, the output impedance at mid-frequency is compensated in a closed-loop manner such that the overall PDN impedance of FDMS power delivery system in the mid-frequency band is low, e.g., below the target impedance. In a similar manner, the high-frequency power supply can be implemented with a high-bandwidth, low-dropout voltage regulator. The output impedance is controlled to be one to two orders of magnitude lower than an on-die decoupling capacitors of the same size. The LDO and/or the buck VR are both powered from a separate rail at the input that runs at a higher voltage than the output.

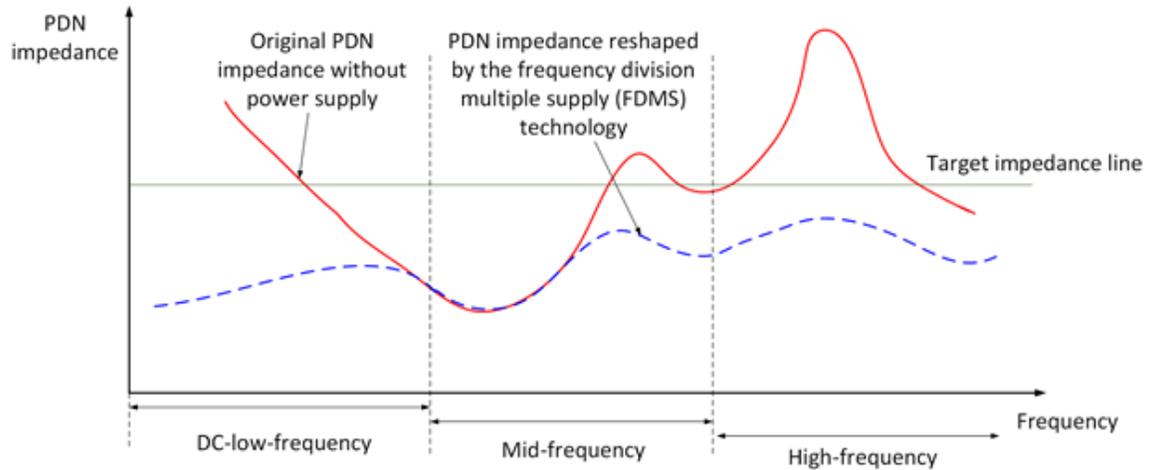


Fig. 7: Frequency response of PDN impedance, before and after shaping by FDMS

Fig. 7 illustrates a comparison between the frequency responses of the PDN impedance with and without FDMS. Prior to FDMS, the impedance without the power supply (red line) violates the target impedance specification at the low, mid, and high frequency bands. With FDMS (dotted-blue line), the PDN impedance is controlled below target impedance across the entire spectrum. Because both mid- and high-frequency supplies serve AC power in their associated frequency bands, the overall efficiency is very close to the efficiency of the DC–low-frequency supply. The loop bandwidth is effectively raised to a much higher value.

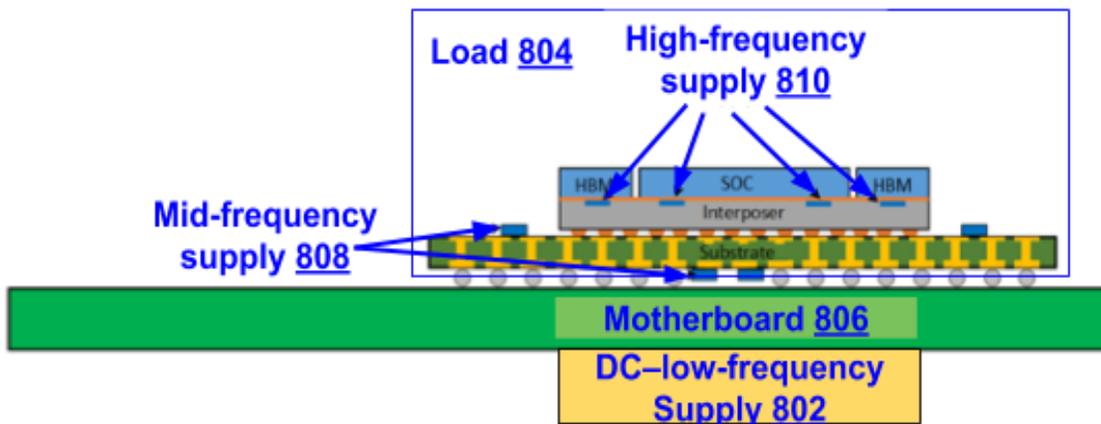


Fig. 8: A physical layout for FDMS

Fig. 8 illustrates a physical layout for FDMS. The DC–low-frequency power supply (802) is mounted on the motherboard (806) vertically below the load (804). Alternately, the DC–low-frequency power supply can be mounted to the side of the load. Thus, DC–low-frequency power is delivered to the ASIC load laterally or vertically. The mid-frequency supply (808) is distributed and integrated onto the processor package. To accommodate the height of the mid-frequency power supply, holes may be cut on the motherboard as appropriate, and the mid-frequency supply can be mounted on the bottom side of the package. The high frequency supply (810) can be integrated with the processor die or silicon interposer.

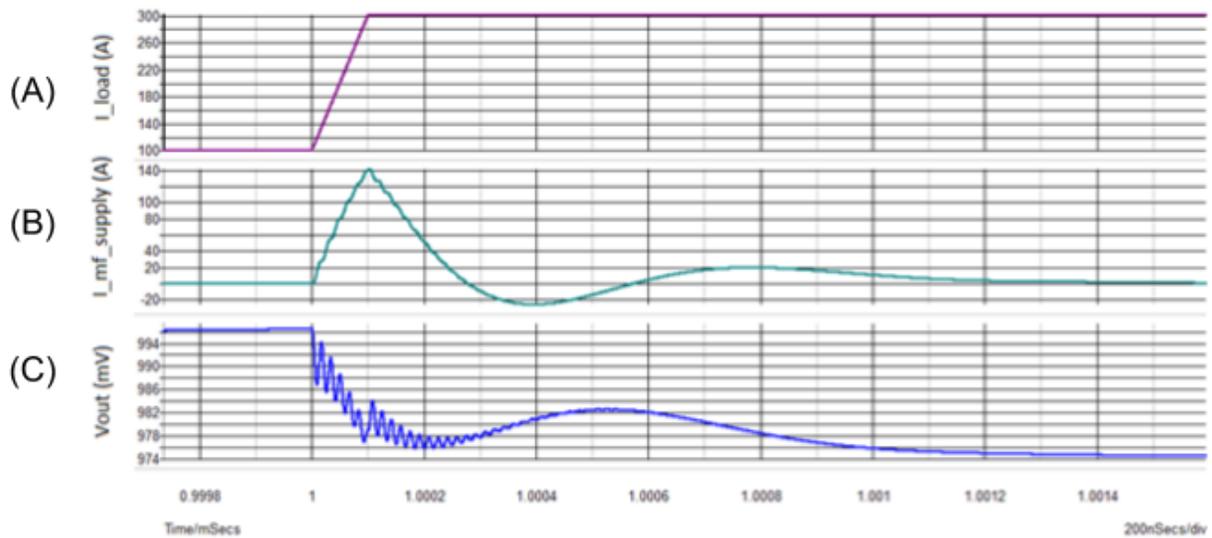


Fig. 9: Time-domain transient responses of a FDMS: (A) A step jump in load current demand (B) Response as measured by package capacitor current (C) Response as measured by power supply output voltage

Fig. 9 illustrates the excellent transient power delivery behavior of FDMS. A step jump in current demanded by the load occurs (Fig. 9A). The load transient in this case being of bandwidth less than 10 MHz, the DC–low-frequency supply and the mid-frequency supply both respond, supplying adequate current to meet the demands of transient current (Fig. 9B). As

compared to a traditional (single-supply) PDN, the transient voltage droop and oscillations are both significantly reduced.

CONCLUSION

This disclosure describes a power delivery network comprising an ensemble of three or more power supplies optimized to differing frequency ranges. A power supply from the ensemble automatically kicks in when transient currents arise with a bandwidth that includes the frequency range of the power supply. Power is delivered across the entire ASIC bandwidth at optimal efficiency and with excellent transient response.