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Multi-layered power module for vertical power delivery applications

ABSTRACT

Voltage regulators (VR), the source of power to printed circuit boards (PCB) and their components, are typically placed laterally with respect to their loads. A VR is typically connected to its load via a power delivery path that comprises metal planes, vias, decoupling capacitors, etc. Powerful ASICs are energy-intensive, consuming hundreds of amperes. This high power consumption leads to unacceptably high power loss on the lateral power delivery path, leading to other undesirable effects such as high operating temperatures and reduced reliability.

This disclosure describes a PCB design that places the VR directly below its load. A vertical power delivery module integrates the VR and passive decoupling capacitors in layered form. The design results in lower power loss, and by virtue of the combined capacitor-VR structure, lends itself to better manufacturability and transient performance. It also provides the designer flexibility in circuit board floor planning and component placement.

KEYWORDS

- Power delivery network
- Voltage regulator
- Vertical power delivery
- Decoupling capacitor
- Layered voltage regulator
- Printed circuit board (PCB)

BACKGROUND

Voltage regulators (VR), the source of power to printed circuit boards (PCB) and their components, are typically placed laterally with respect to their loads. Examples of loads include integrated circuits, ASICs, CPUs, GPUs, resistive components, or any component that consumes electrical energy. A VR is typically connected to its load via a power delivery path that comprises, e.g., metal planes, vias, plated through holes (PTH), lumped elements such as decoupling capacitors, etc. Powerful ASICs are energy-intensive, consuming hundreds of amperes. This high power consumption leads to unacceptably high power loss on the lateral power delivery path, leading to other undesirable effects such as high operating temperatures and reduced reliability.

A related issue in PCB design is the limited flexibility in floor planning and component placement in the plane of the PCB, e.g., in the X-Y directions. The Z-direction, the direction perpendicular to the plane of the PCB, is relatively unhindered in terms of component placement.

Vertical power delivery, e.g., placement of the VR directly below its load, can potentially address the problems of both low thermal efficiency and floor planning. However, the region below the load, e.g., between the load package and the system board, on the reverse side of the system board, or in both locations, is often occupied by decoupling capacitors that serve to improve transient power delivery response. A simple relocation of the decoupling capacitors in order to make space for vertical VRs damages the transient behavior and the integrity of the power delivery network, violating noise or minimum voltage specifications.

DESCRIPTION

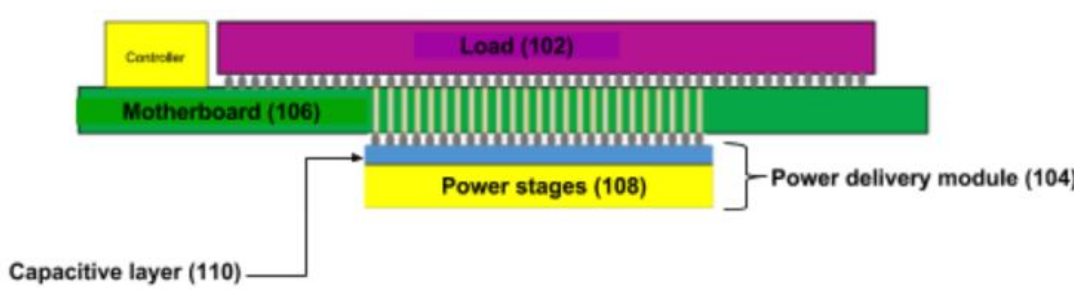

Fig. 1: Vertical power delivery

As illustrated in Fig. 1, per the techniques of this disclosure, the voltage regulator, also known as power stages (108), is encapsulated within a power delivery module (104) and placed directly (vertically) underneath its load (102), e.g., underneath the motherboard (106), between the load package and the motherboard, or otherwise vertically opposed to the load. Passive decoupling capacitors (110) are integrated into the power delivery module, such that the components of the VR and the decoupling capacitors are structured as layers within the power delivery module.

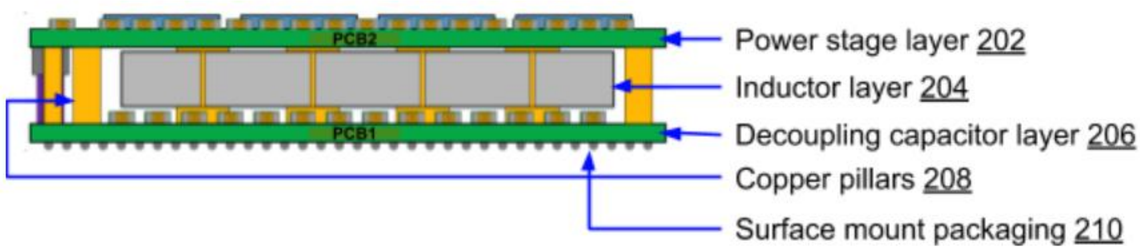

Fig. 2: Layered structure of the power delivery module

Fig. 2 illustrates in finer detail the layered structure of an example power delivery module, where VR components and decoupling capacitors are structured as PCB layers. One of the PCB layers (PCB2) hosts VR components such as power FETs, and is referred to as the power stage layer (202). The decoupling capacitors (206) are placed on another PCB layer (PCB1), possibly a layer relatively close to the load in the vertical stack-up. Other components, such as coupled inductors (204), are placed in the spacing between the layers. The different layers are electrically connected together using copper pillars (208), forming a module. The module as a whole may be molded for mechanical stability. The bottom side of the module can host surface mounts (210), e.g., ball grid array (BGA), land grid array (LGA), or other patterns that match the pad pattern of the load package or the motherboard, depending on where the module is to be soldered.

The layer with decoupling capacitors functions effectively as a bank of charge storage. When the load has a transient demand, charge within a certain range of frequencies is supplied by the capacitors on this layer, mitigating voltage variations at the supply rail. The PCB design rules on this layer are relatively tight, such that the capacitors get densely packed. Compared to direct placement of capacitors at the bottom of the load package or the motherboard, more capacitance fits into a given area when capacitors are arranged in PCB layers within a power delivery module, as described herein. The capacitive layer is designed to minimize series inductance and resistance. The layer also serves as a physical design translation layer, as one side has high density pins to be connected to the load package or motherboard, while the other side has coarser pads to be connected to layers within the power delivery module (such as the VR layer).

The integration of the decoupling capacitors and VR into one vertical power delivery module renders an interposer structure unnecessary. The power delivery module is directly mounted on the reverse side of the load as a common component. The modules can be fabricated and tested independent of the system assembly process, and only modules known to be good are shipped to system-building plants. In this manner, compared to approaches that require interposers and VRs to be individually assembled, the manufacturing process described herein is simpler.

The module itself meets mechanical, structural, and thermal standards, e.g., rigidity, surface planarity, and thermal resistance. The system-level mechanical and thermal design using these modules is therefore simplified as well. With the bank of high-density decoupling capacitors and their associated low inductance/resistance, the transient electrical performance is on par with or better than a lateral power delivery network with decoupling capacitors directly mounted to the load package or board.

To achieve further reductions in size, e.g., for mobile device applications, the following techniques can advantageously be used. Instead of soldering the capacitors to the surface of the PCB, the capacitors can be embedded within the PCB. In addition to traditional multilayer ceramic capacitors (MLCCs), non-traditional capacitor types, e.g., multi-terminal integrated passive device (IPD) capacitors, can be used to further lower inductance and resistance.

CONCLUSION

This disclosure describes a PCB design that places the VR directly below its load. A vertical power delivery module integrates the VR and passive decoupling capacitors in layered form. The design results in lower power loss, and by virtue of the combined capacitor-VR structure, lends itself to better manufacturability and transient performance. It also provides the designer flexibility in circuit board floor planning and component placement.