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FPI SLAVE/12C MASTER BUS MUXING

HP INC

FPI Slave / I2C Master Bus Muxing

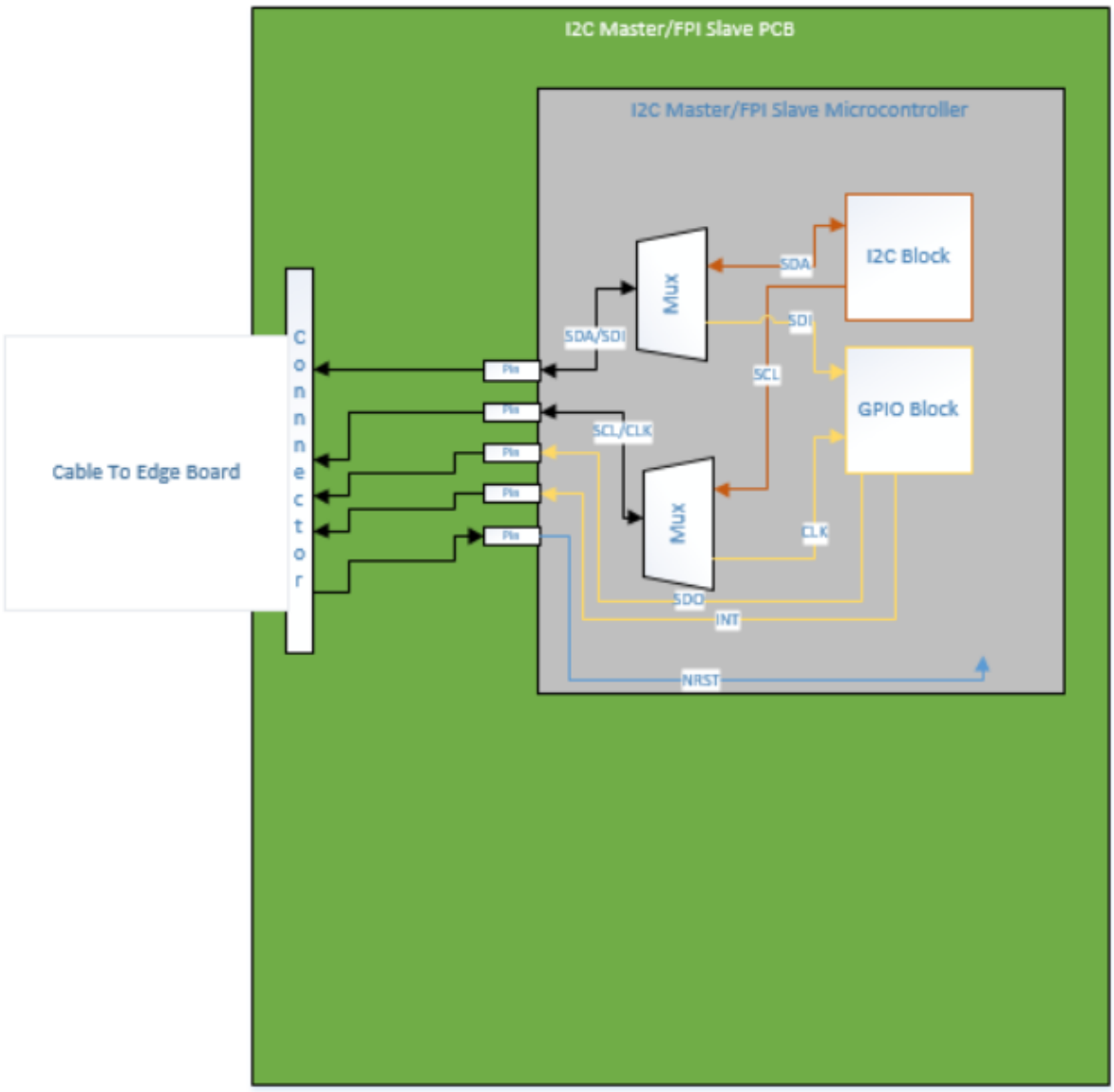
Abstract

Disclosed is a multiplexing scheme that allows the FPI (Front Panel Interface) protocol and the I2C (Inter-Integrated Circuit) protocol to exist on the same bus, without contention between the FPI Master, the FPI Slave/I2C Master, and the I2C Slave. It includes both the necessary hardware and the communication scheme itself to be implemented in firmware.

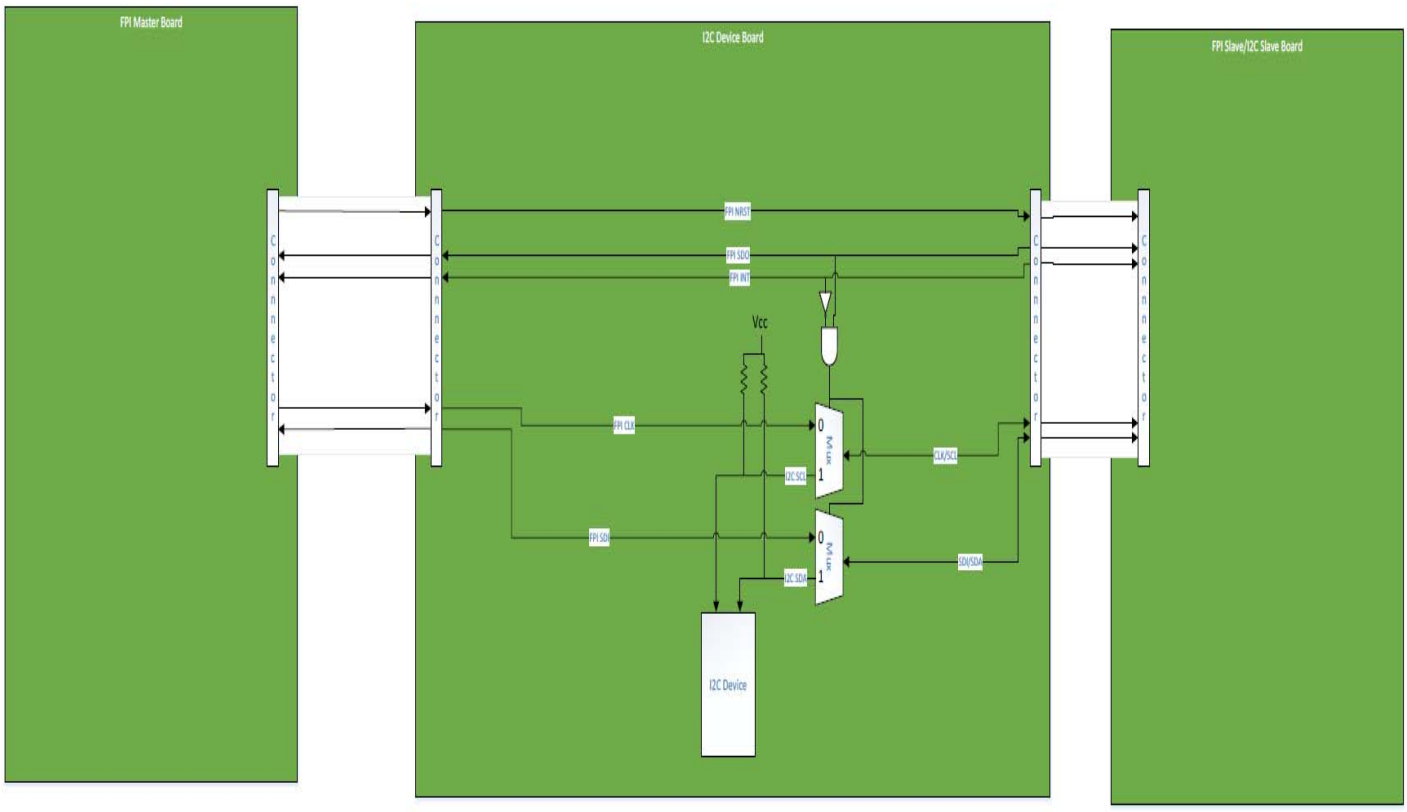
Description

The current FPI interface has 5 signals: Clock (CLK), Serial Data In (SDI), NReset (NRST), Interrupt (INT), and Serial Data Out (SDO). These signals are with respect of the FPI Slave/I2C Master. The I2C interface protocol has 2 signals: Data (SDA) and Clock (SCL). Both protocols are Master/Slave interfaces. Normally, the FPI Slave (in our case a microcontroller, MCU) would need to have dedicated pins for all 7 of these signals. However, with this interface the MCU can internally mux the SDI line with the SDA line and the CLK line with the SCL line. There will also be external muxing that split up the FPI signals (CLK and SDI) and the I2C signals (SDA and SCL), that allow each of the signals to be directed to their respective destination. These externally muxed signals will be controlled by the SDO and INT lines by the FPI slave. These SDO and INT lines will be fed through an inverter and an AND gate to control the select lines of the demultiplexing. Pull up resistors must be added to the SDA/SCL lines to stay aligned with I2C protocol. Below is a diagram of the hardware for both the internal and external muxing

Muxing Scheme on I2C Master MCU



Muxing Scheme on I2C
Device Board

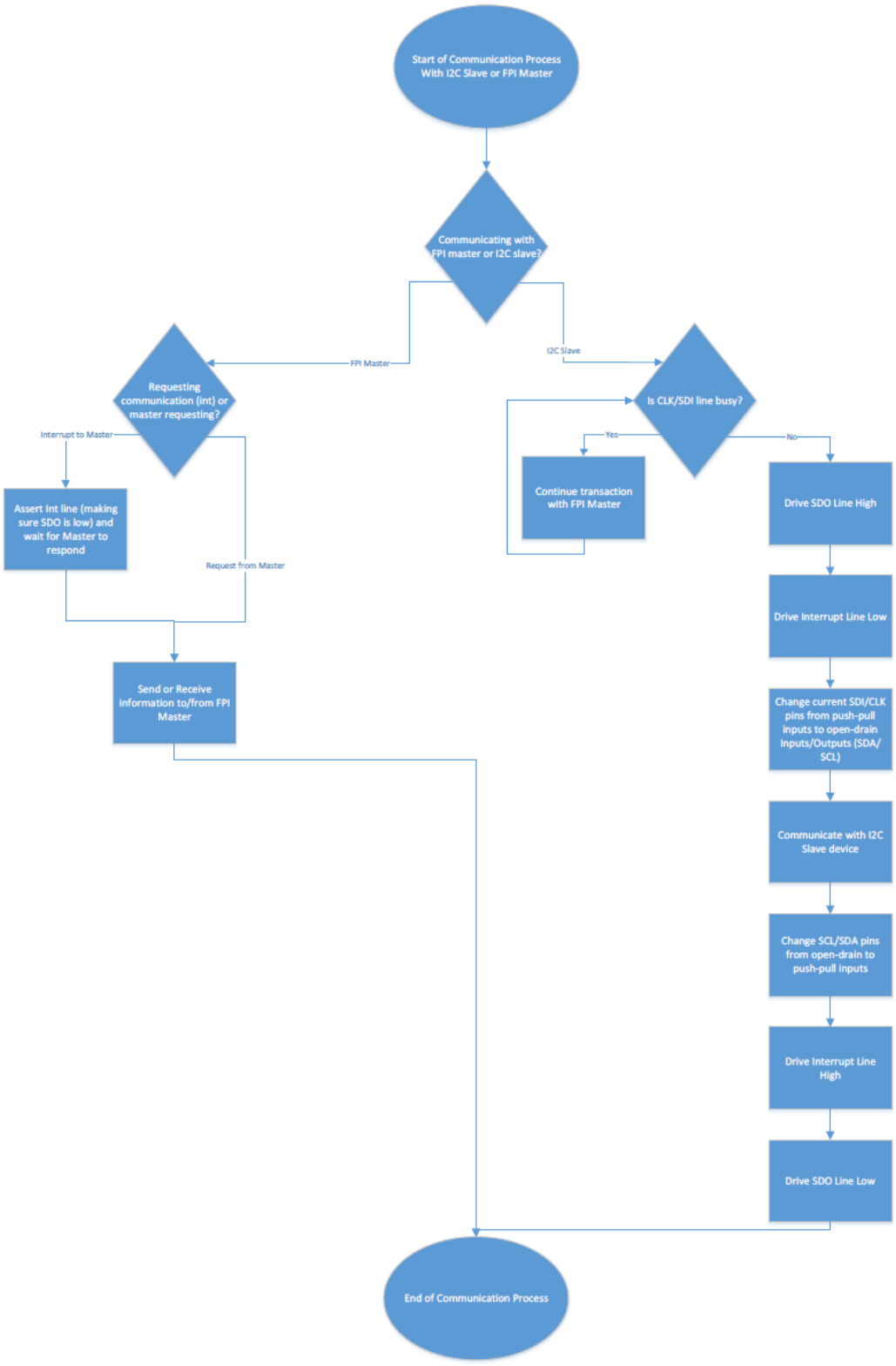


The default mode of the FPI Slave/I2C Master will be FPI Slave, until it is necessary for the FPI Slave to become the I2C Master and initiate a conversation with I2C Slave. This will be done by having the FPI Slave first assert it's SDO line high. This will let the FPI Master know that the slave is busy. Lastly, the FPI slave will assert the INT line (active low), causing the external muxing to switch from the FPI lines to the I2C lines. Normally the asserted INT line would cause the FPI Master to query the Slave, however since the Slave asserted it's SDO line high to let the FPI Master know it would be busy, it should not get queried from the FPI Master. At this point, the FPI slave will change its current FPI SDI/CLK pins from push-pull inputs to open drain I/Os, and then begin communication with the I2C slave. Once communication has been finished between the I2C Master and the I2C Slave, the I2C Master will change it's pins back to push-pull inputs, de-assert the interrupt line, and finally de-assert the SDO line. At this point when the SDO line has been fully de-asserted, the FPI slave should be ready to be communicated with by the FPI master.

It is necessary to include the external muxing on the SDA/SDI and SCL/CLK bus because the I2C interface does not necessarily have a way to deal with a false start condition. If there is communication going on between the FPI Master and FPI slave with no external muxing, the I2C slave could be put into an unknown state due to the bus activity and cause problems when being addressed in future transactions.

Below is a control flow diagram describing the FPI Master/I2C Slave Communication process.

FPI Slave/I2C Master Control Flow Diagram



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