VERTICAL POWER DELIVERY STRUCTURE FOR ULTRA-HIGH CURRENT APPLICATIONS

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VERTICAL POWER DELIVERY STRUCTURE FOR ULTRA-HIGH CURRENT APPLICATIONS

BACKGROUND

Current processing unit applications in large-scale data centers are trending toward ultra-high current (e.g., greater than 1000 Amperes (A)) and high power.

SUMMARY

This document describes a vertical power delivery structure for ultra-high current processing unit applications. In some cases, the structure includes a hollow interposer to interface with point-of-load (PoL) voltage regulator (VR) modules with a motherboard. The VR modules can include output power pins located on a peripheral thereof such that electrical connections are not needed in a center area beneath the VRs. As a result, this allows removal of interposer material located beneath the VRs with hollow space. Therefore, high frequency decoupling capacitors can be placed on the motherboard bottom inside the interposer hollow. The interposer will adapt the VR power pin-out to the BGA land patterns of the motherboard.
DESCRIPTION OF DRAWINGS

Figure 1 is a cross-sectional view of an example architecture including multiple PoL VR modules.

Figure 2 illustrates an exploded view of the architecture of Figure 1.

Figure 3 illustrates a bottom view of the architecture of Figure 1.

Figure 4 illustrates a bottom transparent view of the architecture of Figure 1 including decoupling capacitors.

Figure 5 illustrates a cross-sectional view of an example architecture including a single PoL VR module.

Figure 6 illustrates an exploded view of the architecture of Figure 5.

Figure 7 illustrates a bottom view of the architecture of Figure 5.

Figure 8 illustrates a bottom transparent view of the architecture of Figure 5 including decoupling capacitors.

DETAILED DESCRIPTION

Traditional power delivery technology places the point-of-load voltage regulator (PoL VR) on the side of the processor unit such that power is delivered laterally to the processor. However, by doing so, a voltage drop (IR drop) across the PCB power plane resistance is proportionally increased with the processor current. Additionally, the IR drop associated with copper conduction losses are increased exponentially. This results in not only an excessive amount of wasted energy but also significant challenges to dynamic voltage regulations of the processor.
To address this power delivery problem along with increasing processor current demand, this document discusses moving the PoL VR underneath the processor -- either on the bottom side of the motherboard or on the bottom of the processor package substrate. As a result, power delivery from the VR to the processor will be on a reduced length-vertical path with significantly reduced impedance (e.g., 3 times or greater reduction).

Furthermore, as compared to co-packaging of the VR with the processor chip, mounting the VR on the bottom of the motherboard PCB can provide lower complexity, higher reliability, and lower cost in terms of electrical design, manufacturing assembly yield, and thermal management. Furthermore, as a result of the constrained space in the motherboard PCB under the processor, a high density of the VR is preferred. Therefore, this document discusses an on-board vertical power delivery structure based on a hollow interposer with high density PoL VRs. That is, this document discusses that power can be vertically delivered from VR components to the processor through a (short) low impedance path, while including distribution of the decoupling capacitors on the motherboard bottom.

Figure 1 illustrates a cross-sectional view of an example architecture including multiple PoL VR modules. The architecture includes a motherboard coupled to a xPU chip, a front stage VR, PoL VRs, and PoL VR interposers. Specifically, the architecture includes three PoL VRs coupled to the motherboard, with interposers connected between the PoL VRs and the motherboard including interposer hollows between the PoL VRs and the motherboard. Additionally, the interposer hollows can include decoupling capacitors (“decaps”); and further other decoupling capacitors can be coupled to the interposers.
Figure 1 illustrates an exploded view of the architecture of Figure 1.

Figure 2 illustrates an exploded view of the architecture of Figure 1.
Figure 3 illustrates a bottom view of the architecture of Figure 1.

![Figure 3](image)

Figure 3

Figure 4 illustrates a bottom transparent view of the architecture of Figure 1 including the decoupling capacitors.

![Figure 4](image)

Figure 4
Figure 5 illustrates a cross-sectional view of an example architecture including a single PoL VR module. The architecture includes a motherboard coupled to a xPU chip, a front stage VR, a single PoL VR, and PoL VR interposers. Specifically, the architecture includes a single PoL VR coupled to the motherboard, with interposers connected between the PoL VR and the motherboard including interposer hollows between the PoL VR and the motherboard. Additionally, the interposer hollows can include decoupling capacitors (“decaps”).

![Figure 5](image)

Figure 6 illustrates an exploded view of the architecture of Figure 5.
Figure 7 illustrates a bottom view of the architecture of Figure 5.
Figure 8 illustrates a bottom transparent view of the architecture of Figure 5 including the decoupling capacitors.

Figure 8

ABSTRACT

This document describes a vertical power delivery structure for ultra-high current processing unit applications. The structure includes hollow interposer to interface with point-of-load (PoL) voltage regulator (VR) modules with a motherboard. High frequency decoupling capacitors can be placed on the motherboard bottom inside the interposer hollow.