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# Data Transfer to Non-volatile Memory (or Persistent Memory) During Input Power Loss

Rama Prasad Atluri
*Hewlett Packard Enterprise*

Mark A. Lawrence
*Hewlett Packard Enterprise*

Daniel Humphrey
*Hewlett Packard Enterprise*

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## 1.0  Abstract:

In a critical server losing its input voltage/power, the server goes down after 10/20ms of hold-up time. In these hold-up time the data need to be transferred from volatile memory to non-volatile memory (NVDIMM). For years this process is being done successfully, by transferring the data during this 10/20ms hold-up time. However, this process is having the disadvantage of the server going down for each and every event of input power loss using NVDIMMs platforms.

To overcome this disadvantage, a new method or technique is proposed in this publication/disclosure (Fig 1). The proposed technique utilizes the signal (called bulk voltage). Whenever, the energy levels (called bulk voltage) in a power supply becomes low, the server starts transferring the data (compared to each loss of input power earlier) to non-volatile memory reducing the number of shut downs of the server. If the input power loss duration is from 10ms to 80ms depending upon the load on the server, the shutdown of the server can be avoided completely.

The cost of this feature is miniscule compared to the cost of adding UPS/mega cell/Super cap in each and every server/platform.
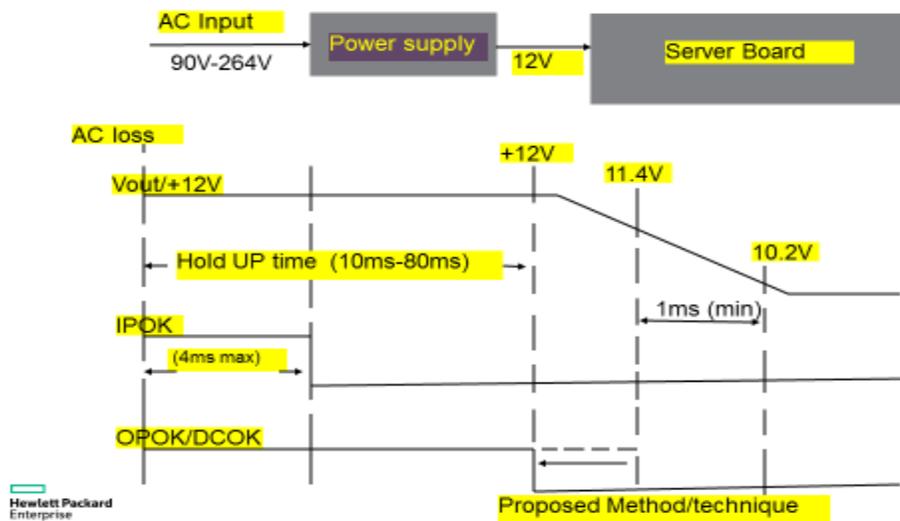
Figure 1: The proposed power architecture and its waveforms with loss of ac input

## 2.0   Description of the Prior Art:

In general, backup of the data in a server is being done either using either UPS (Fig 2) or some kind of battery cell (i.e. Mega cell, super cap etc.). These units occupy a lot of physical space in a server and provide the good data protection in case of input power loss to the server. However, the main disadvantage of these UPS/Mega cell/super cap units are their size and cost.

The main purpose of this publication/disclosure is to provide a solution for customers not having UPS in their operating infrastructure, and to have a data protection (using NVDIMMs) from the loss of ac input (Fig 1).

NVDIMMs require minimum 10.2V at its input connector terminal. Power supply delivers its output voltage at the output connector. The voltage drop from power supply connector to NVDIMM connector need to be taken care of while powering up the NVDIMM. Existing solutions utilize the hardware assisted ADR scheme which requires ~100uS time and can be met relatively easy (Fig 1 of 1ms).

Another prior solution is enabling the PCODE assist ADR process with AEP DIMMs for each and every ac input loss. Basically for any small duration (even <5ms) of ac input glitch will shut down the server and re-boot. This may cause customer irritation nuisance interruption of the process. This can be avoided with the proposed technique.

However, recently for Apache Pass (AEP) DIMMs, a PCODE assisted ADR is a requirement.   PCODE assist ADR prevents loss of data with AEP NVDIMMs and has benefits compared to hardware ADR process.

With input ac loss, PCODE assist ADR process with AEP NVDIMMs require input voltage >10.2V for 3-4ms at the NVDIMM connector. The technique proposed in this disclosure is shown in Figure 1. Using this technique, AEP NVDIMMs work efficiently without losing any data in PCODE assist mode ADR process and also reduces the number of server shut downs considerably.
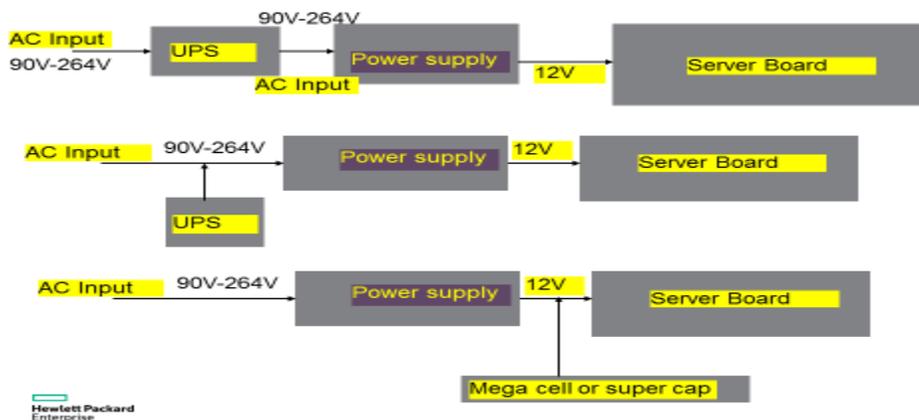
Figure 2:    Data Transfer using UPS/mega cell/Super Cap –Prior Art

## 3.0    Description of the proposed method or technique:

In general, backup of the data in a server is being done either using either UPS or some kind of battery cell (i.e. Mega cell, super cap etc.). These units occupy a lot of physical space in a server and provide the good data protection in case of loss of input power to the server. However, the main disadvantage of these UPS units is its size and cost.

The purpose of this disclosure is to provide a solution for customers not having UPS in their operating infrastructure and to have a data protection (using NVDIMMs) from the loss of ac input.

NVDIMMs require a minimum 10.2V at its input connector terminal. Power supply delivers its output voltage at the output connector. The voltage drop from power supply connector to NVDIMMs connector need to be taken care of while powering up the NVDIMM. Existing solutions utilize the hardware assisted ADR scheme which requires ~100uS time and can be met relatively easy.

However, for recent Apache Pass (AEP) processor, a PCODE assisted ADR is a requirement. PCODE assist ADR prevents loss of data with AEP DIMMs and has benefits compared to hardware ADR process.

A new method or Technique is proposed in this disclosure/publication (Figure 1).  The proposed technique utilizes the signal of the bulk voltage levels inside the power supply. Whenever, the energy levels (called Bulk Voltage) in a power supply comes to certain level or value, the power supply OPOK signal output goes low (from high).  Once the OPOK signal is low, the server is expected to start transferring the data (compared to

each loss of input power earlier) to non-volatile memory reducing the number of shut downs of the server.

If the input power loss duration is from 10ms to 80ms depending upon the load on the server, the shutdown of the server can be avoided completely.

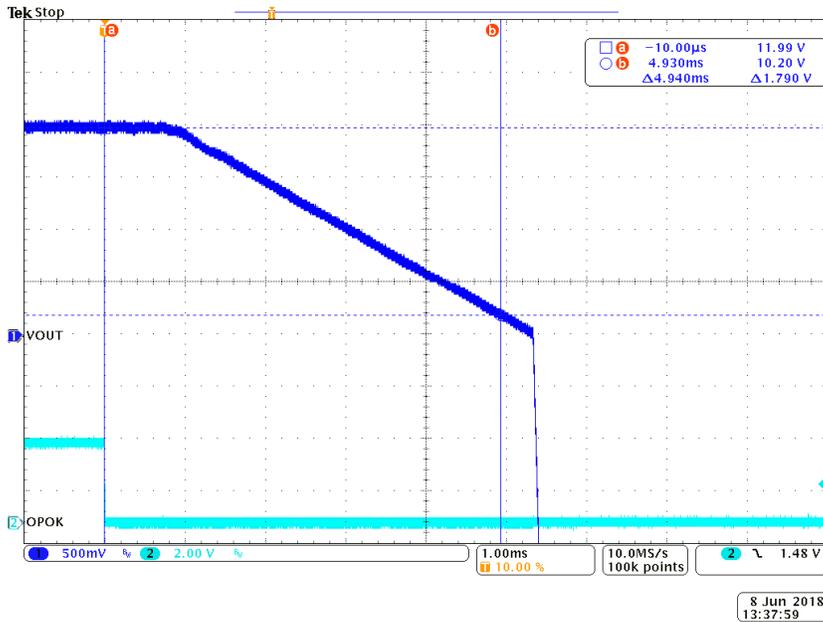Figure 3 shows the waveform for power supply with the proposed technique or method.



Figure 3:     proposed method/technic implemented waveform with simple FW update

## 4.0   Conclusion:

With input ac loss PCODE assist ADR process with AEP NVDIMMs require input voltage >10.2V for 3-4ms at the NVDIMM connector. The technique proposed in this publication/disclosure is shown in Figure 1. The proposed technique for AEP NVDIMMs work efficiently without losing any data in PCODE assist mode ADR process and also reduces the number of server shut downs considerably (Fig 1).