August 20, 2018

MULTI-STAGE 48V TO POINT-OF-LOAD (POL) POWER ARCHITECTURE FOR ULTRA-HIGH CURRENT PROCESSING UNIT APPLICATIONS

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ABSTRACT

This document describes a multi-stage power architecture as applied to 48V, ultra-high current applications. The multi-stage system can provide high power density within a small footprint and support high-current operations by decoupling the density, efficiency, and bandwidth requirements of the last stage supplying input to the voltage regulator for the PoL from the other stages of the architecture that supply input to the rest of the voltage regulators on the board. The described multi-stage system is more cost and resource-efficient than currently available power architectures, and can be implemented within smaller and smaller processing unit applications with increasing power density requirements.

DESCRIPTION

This document describes techniques for an improved high density, high bandwidth, and high efficiency voltage regulator stage for powering high-current electronics, such as CPUs, GPUs, neural processing units (NPUs), tensor processing units (TPUs), or vision processing units (VPUs), collectively known as xPUs. Current xPU applications in large-scale data centers are trending toward ultra-high current (typically around1000A) and high power. However, the size of the motherboard and the xPU does not increase proportionally with current and power, creating increasingly high demand for dense power solutions. In particular, the voltage regulator next to the xPU must be able to deliver ultra-high current and high power under tight space constraints in order to fit within the footprint available.

Existing power architectures utilize a transformer-based high-ratio converter and then a low-voltage voltage regulator at the PoL. Limitations associated with this approach include the high cost, long lead time to market, and reduced scalability associated with highly customized

solutions such as transformer-based converters. Additionally, a single high-ratio bus converter cannot be placed at the front-end of a motherboard, because it is physically far from the PoL (e.g., a processing unit), and because a 6V bus is not suitable for power distribution across the entire motherboard as the current is too high. Furthermore, a single bus converter may not be suitable for supplying power to the entire motherboard, as there are other loads with different voltage and power density requirements.

To minimize the distance between the voltage regulator and the processor and satisfy physical constraints, it is often desirable to place the voltage regulator directly underneath the processor—either on the bottom side of the motherboard or on the bottom of the processor package substrate. In addition to providing high-density solutions with high-density powertrains, voltage regulator technology must also feature high-density output decoupling capacitors to suppress high-frequency noise in power supply units, as decoupling capacitors with small outputs require high loop bandwidth of the voltage regulator. It is a design goal in many applications to achieve high power conversion and power delivery efficiency for the best total cost of ownership. Considerations within the total cost of ownership can include, for example, ease of cooling, energy efficiency, etc.

With the rise of ultra-high current and high power processing applications, there is a corresponding increase in demand for an ultra-high current, high power xPU power delivery system, such that the voltage regulator stage—located at the PoL—features high density, high bandwidth, and high efficiency. Multi-stage power architecture is a compelling choice in existing 48V systems, as the multiple stages decouple the density, efficiency, and bandwidth requirements of one stage from the other stages. For example, the heightened specification

requirements of the last conversion stage at a voltage regulator can be decoupled from other front-end, intermediate conversion stages.

The improved system uses a relatively low input voltage (e.g., <6V) in the last stage voltage regulator at the PoL to facilitate using more advanced technology at the node, such as monolithic driver MOS (metal-oxide semiconductor) technology, so that a higher switching frequency for the voltage regulator can be used to provide higher density and to control bandwidth. However, there are challenges associated with front-end intermediate power conversion stages within a multi-stage power architecture that must be resolved in order to effectively use low-voltage voltage regulators for xPU power delivery. For example, if a single 48V-to-6V intermediate bus converter was used to generate input to the last stage voltage regulator at the PoL, distribution would be challenging because 6V is too low to be used due to the high current at board-level (e.g., 100A for 600W). Alternatively, if the 48V-to-6V intermediate converter was moved to be next to the last stage voltage regulator, there would likely be space issues, as the converter may not fit on the board. In addition, it can be impractical to deliver a single 6V bus to all downstream loads, as some system loads (e.g., DDRs, BMCs, other logic devices, etc.) on the motherboard do not require high-density, low-voltage voltage regulators like the xPU processors do.

FIG. 1 illustrates an example of the new multi-stage power conversion architecture as applied to datacenter server boards.

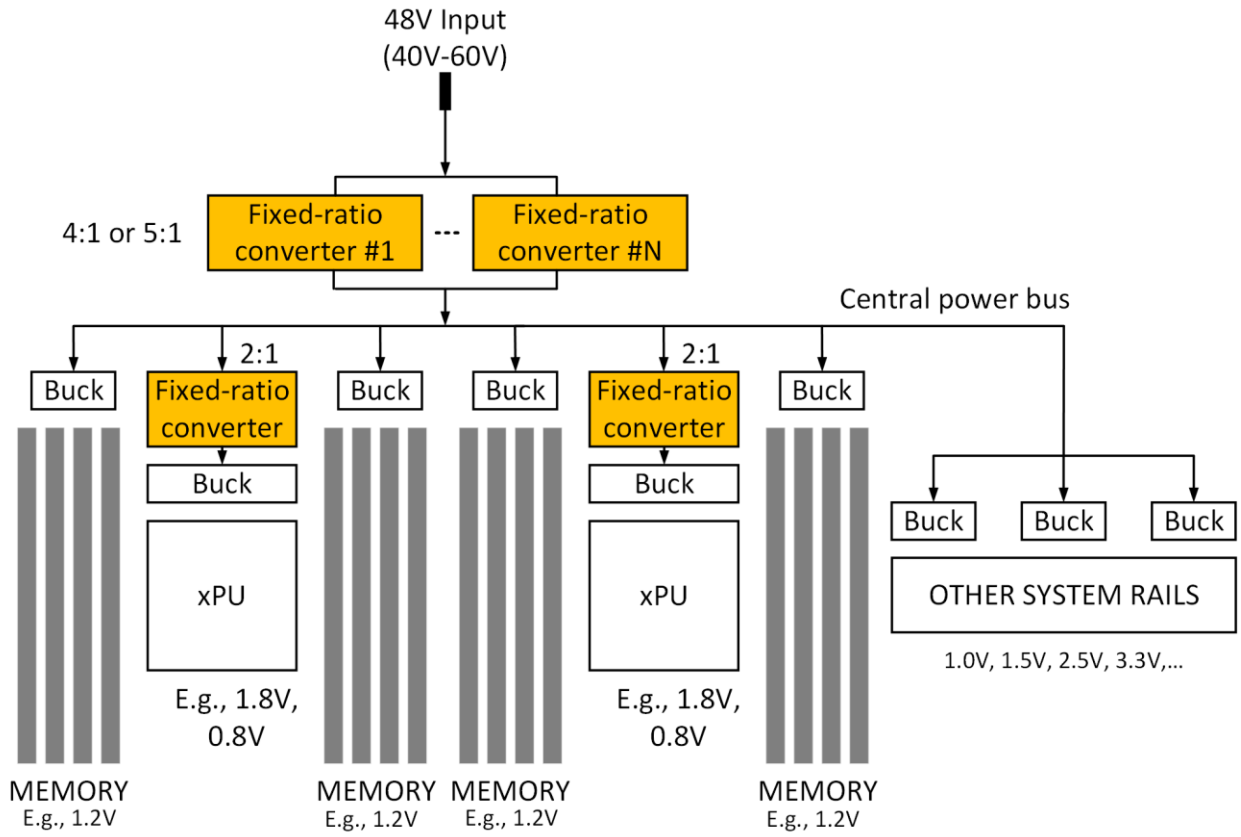

FIG 1. Multi-stage 48V-to-PoL power architecture for ultra-high current xPU applications

In this multi-stage architecture, a fixed-ratio intermediate bus converter (e.g., 4:1 or 5:1) is being used to convert 48V input (40V-60V) to an intermediate bus voltage (e.g., 10V-15V for 4:1, 8V-12V for 5:1). This intermediate bus is distributed across the whole motherboard to supply power to all the downstream voltage regulators. Some applications may have a total power requirement different than what can be provided through a single fixed-ratio converter; in those situations, multiple fixed-ratio converters can operate in parallel to meet the total power requirement.

FIG. 2 shows an example first-stage fixed-ratio converter topology. The first-stage fixed-ratio converter can be based on switched tank converter (STC) topologies and the second stage 2:1 can be based on switched capacitor topologies.

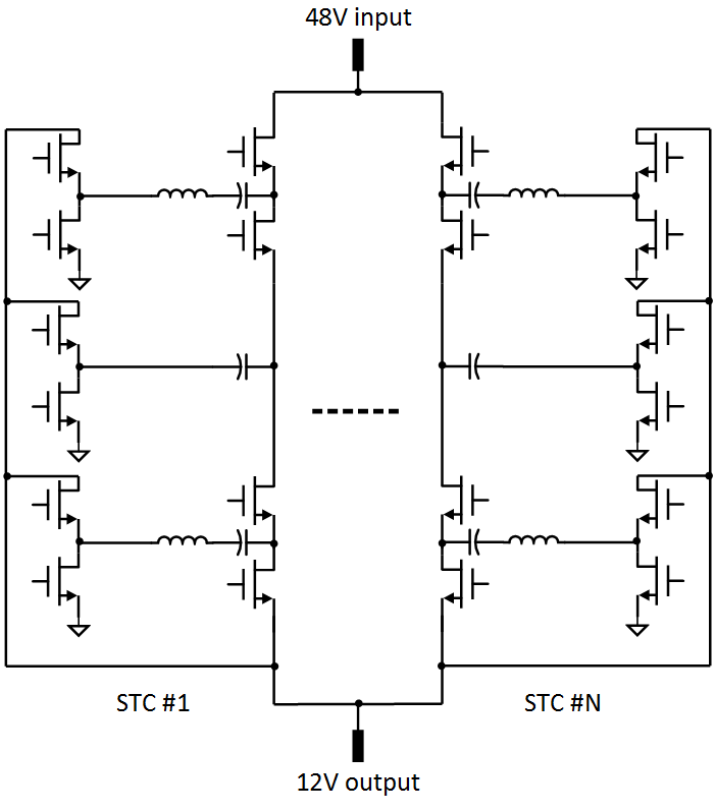

FIG. 2 Example first-stage fixed-ratio converter: a multi-phase 4:1 STC fixed ratio converter

The improved system uses another fixed-ratio converter to meet the high-density, high-efficiency and high-bandwidth requirements of the voltage regulator for the processor (e.g., the xPU core rail). For example, the system can include another 2:1 fixed-ratio converter to step down the intermediate bus voltage by a ratio of 2 so that the voltage regulator for the xPU core rail can utilize low voltage (e.g., 6V) technology. The first-stage 4:1 or 5:1 fixed-ratio converter can have an efficiency of up to 98.5%, the second-stage 2:1 fixed-ratio converter can achieve an efficiency around 99%, and the last stage voltage regulator can have an efficiency of 91%-93% for an 0.8V core rail. The overall efficiency can reach 88.7%-90.6%.

FIG. 3 illustrates an example second-stage fixed-ratio converter topology. The second-stage fixed ratio converter can be based on switched capacitor converter (SCC) topologies.

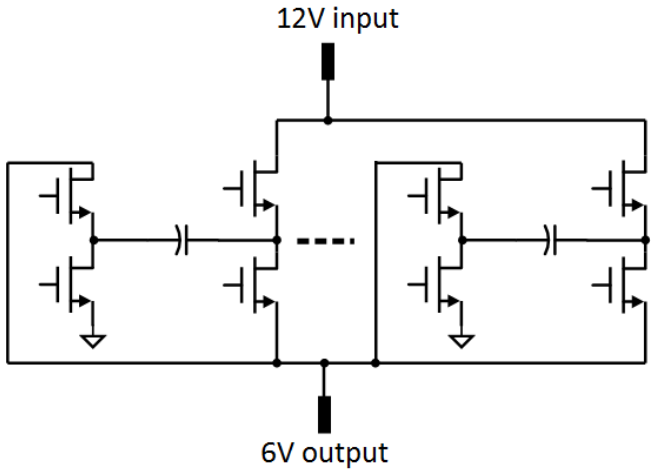

FIG. 3 Example second-stage fixed-ratio converter: a multi-phase 2:1 SCC fixed ratio converter

FIG. 4 illustrates an example layout of the improved multi-stage power architecture. In this particular implementation, the architecture is based on a first-stage 4:1 STC, a second-stage 2:1 SCC, and 6V multiphase buck regulators.

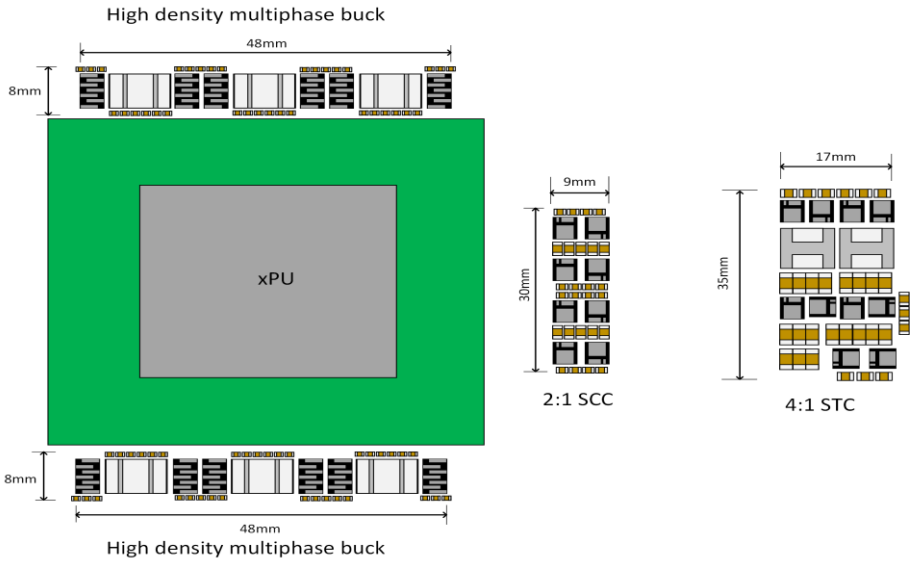

FIG 4. Physical layout of the multi-stage 48V-to-PoL power architecture

There are several advantages of this multi-stage architecture, including the high overall efficiency, the high power density, and the scalability and low cost of the system relative to other solutions. For example, the overall efficiency of a front-end 4:1 fixed-ratio converter cascaded by a 2:1 fixed-ratio converter can achieve a similar efficiency to that of a single 8:1 fixed-ratio converter. The second stage 2:1 fixed-ratio converter features high power density such that it can be easily fit in the local area where the processor sits, reducing size and space requirements for the board on which the system is implemented. The first-stage fixed-ratio converter offers a common intermediate bus that can supply power to all downstream voltage regulators on the board. The improved system offers scalability to different applications and products and has a short lead time due to its discrete component-based design instead of using highly customized designs with integrated magnetics. Additionally, there are large cost and supply chain advantages to implementing and maintaining a discrete multi-stage system—each stage can be individually serviced, replaced, added, etc.