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# Advanced Fan Pinout

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As the requirements for more computational power increases with growing demands for faster data transmission, electronic circuits grow denser and more complex, along with their design effort. Engineers are often tasked with seeking methods to simplify designs to lower cost and provide more affordable solutions to end customers. Finding methods to reduce the pin count of ICs (Integrated Circuits) and transmission lines in PCBs (Printed Circuit Boards) is one method to achieve this goal. An Advanced Fan Pinout (AFP) can help achieve this on a server board's FPGA and Thermal electrical circuitry. The AFP can reduce the number of data transmission lines on the PCB to help alleviate the often encountered problems:

a. A higher pin count equates to a higher number of data transmission lines on the PCB that need to be routed. A denser grouping of transmission lines requires more time to route, which complicates the design and prolongs the design schedule.
b. More transmission lines may contribute to requiring a higher PCB layer count, which also contributes significantly to total design cost.

One current industry implementation, the smart fan pinout, is highlighted in Figure 1 below. Three control signals are used to drive the smart fans. The fan is driven by continuous PWM pulses outputted by the FPGA. When the fan is connected, the power signal is tied, and the PWM outputs a continuous pulse. INSTALL and FAIL are 2 additional input feedback signals that indicate when the fan is installed and indicates when a fan failure event has occurred. The INSTALL and FAIL signals are simple logic high or low level triggered signals inputted to the FPGA to indicate the Fan status.

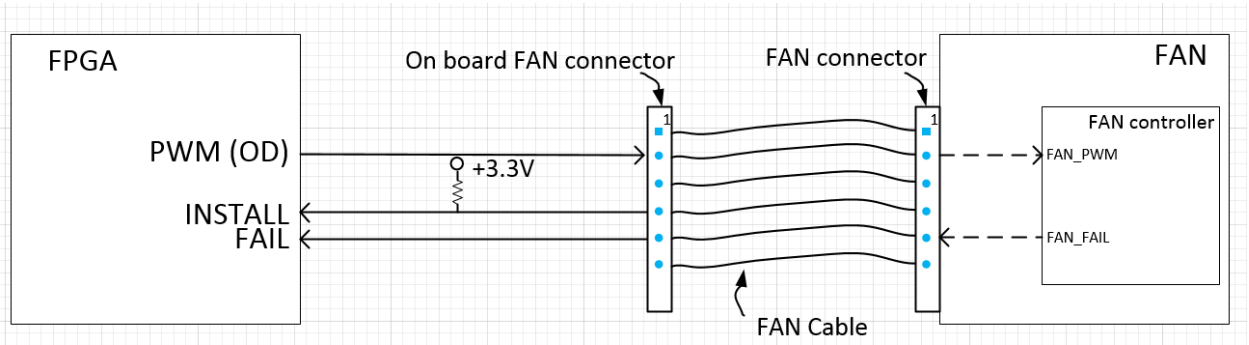


**Fig 1 HPE smart FAN pinout connection**

The proposal illustrated in Figure 2 below is the Advanced Fan Pinout (AFP) concept, where the previous independent Fail and Install signals can be eliminated on the fan cables and fan connectors, while retaining the same desired effects by tying them directly to the

PWM pulses. A modified fan design has additional circuitry built in to help achieve this. When the fan is inserted, the PWM output pin on the FPGA is tied to a power signal and pulses are generated by the FPGA to drive the fan, as in any other fan circuit design. The difference from the smart fan design, is the PWM signal is directly branched off as 2 additional inputs to the FPGA INSTALL and FAIL pins. The FPGA detects the fan presence by programming a filter that detects a sample of pulse widths to indicate the fan presence. During a fan fail event, the fan controller sends out a fan fail signal that activates the MOSFET integrated in the fan, this activates the voltage divider circuit, which causes the amplitude of the PWM pulses to drop. The FPGA decodes a fan fail (only valid with INSTALL present) from the drop in the PWM pulse amplitudes. Figure 3 shows the calculated values for determining a fan fail event. The FAIL amplitude is adjusted to a lower value than the standard PWM amplitude to leave no margin of error for the FPGA. The FAIL signal is monitored as the output voltage from the voltage divider circuit.

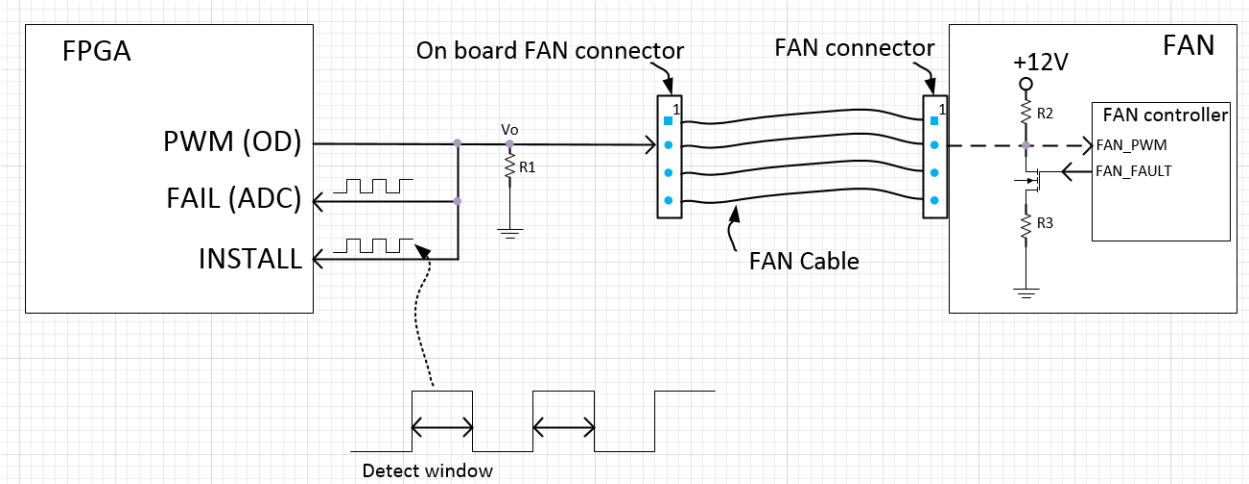


**Fig 2 Advance FAN pinout connection**

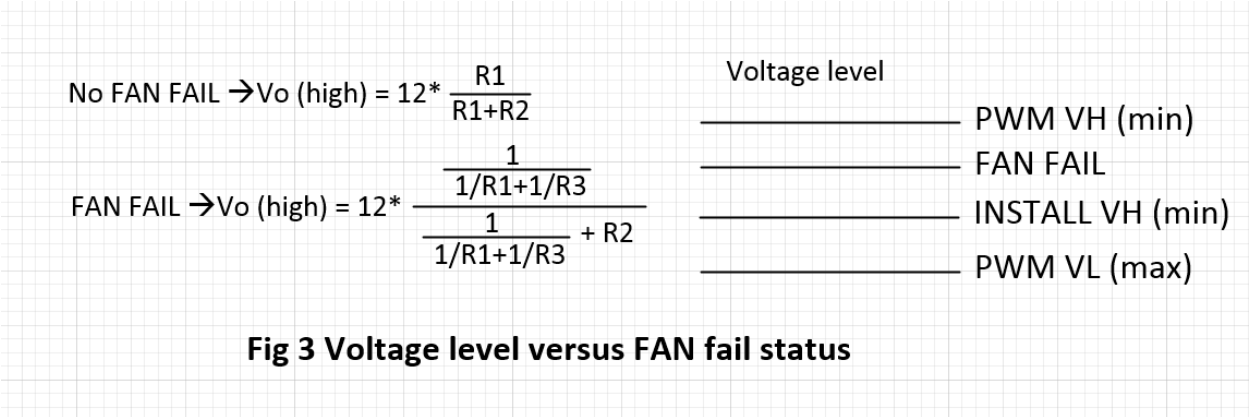


**Fig 3 Voltage level versus FAN fail status**

Utilizing the AFP over the current Smart fan pinout can yield the following advantages:

a. Minimizes the number of data transmission lines required to control fans, lowering design complexity and saving time.
b. Minimizing data transmission lines potentially lowers the PCB layer count, saving design and material costs.
c. Reduces connector pin counts and cable pin outs, which increases spacing between connectors, allowing for better system cable routing.
d. Lower cable and connector pin counts lowers the material costs.

Disclosed by Geoffrey Sun, Peter Liao, Eason Chen and Mealy Cheng, Hewlett Packard Enterprise