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Method And Apparatus For Improved Cumulative Yield Of On-Package Voltage Regulator Assembly

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METHOD AND APPARATUS FOR IMPROVED CUMULATIVE YIELD OF ON-PACKAGE VOLTAGE REGULATOR ASSEMBLY

ABSTRACT

In high-power application-specific integrated circuits (ASICs), multiple voltage regulator ICs are required on the package to provide the required power to the ASIC. These underfill components on package are not reworkable and manufacturing flaws cannot be fixed, thus having a negative impact on the overall package yield. A system and method are proposed here to increase the package yield on ASICs by placing redundant voltage regulator ICs in addition to the multiple voltage regulator ICs operating in parallel on a semiconductor package. The redundancy ensures that the overall system in the package would be functional even with certain limited flawed ICs, which are then disabled. This method increases the cumulative assembly yield, with relatively small increase in cost and size. Furthermore, they allow a degree of freedom in the die size and power rating selection of voltage regulator ICs.

BACKGROUND

In high-power application-specific integrated circuits (ASICs), multiple voltage regulator ICs are required on the package to provide the required power to the ASIC. High-power voltage regulators have multiple ICs on the same semiconductor package, where each one of the ICs provides a portion of the total required power. This is needed because a single IC is limited in the amount of power it can deliver. Thus, multiple ICs operate in parallel and their power is summed and delivered to the ASIC. An example of this implementation is a multiphase buck converter. Since placed on a package, each one of these ICs may require an underfill material, such as epoxy, for better mechanical attachment and reliability. Unlike surface mount components (SMTs), underfill components on the package are not reworkable, and hence manufacturing

flaws cannot be fixed. This has a dramatic negative impact on the overall package yield, which could be unacceptably low. A system and method are proposed here to increase the package yield on ASICs.

DESCRIPTION

A system and method are disclosed here to improve the cumulative assembly yield of the voltage regulator system in a package by placing redundant voltage regulator (VR) ICs in addition to the multiple voltage regulator ICs operating in parallel on a semiconductor package. For example, as shown in FIG. 1, a package with 30 voltage regulator ICs, with each IC having an individual IC assembly yield of 98%, will result in an overall cumulative yield of 55%. With the addition of one redundant IC to it, the overall cumulative yield increases to 87%, while the addition of one more redundant IC increases the cumulative yield further to 97%, which is almost equal to the yield of an individual IC. This is a significant improvement from 55% with less than 10% increase in package bill of materials, cost and area.

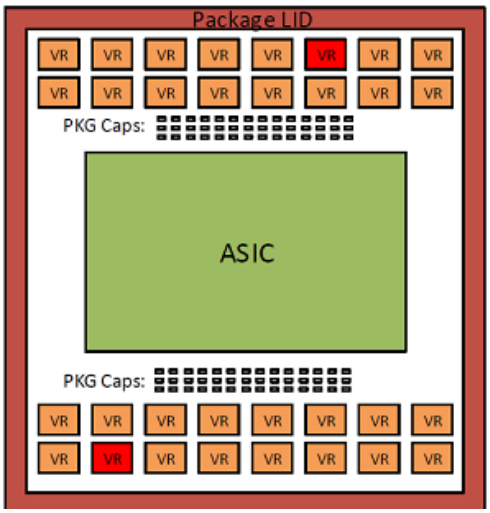

FIG. 1: Semiconductor package with 32 voltage regulator ICs, with two redundant, flawed ICs shown in red

The system and method further suggest placing redundant ICs, so that even with certain limited flawed ICs, the overall system in the package would still be functional. For example, 30 voltage regulator ICs are needed to power the ASIC. With 31 voltage regulator ICs, one flawed IC is allowed, and with 32 voltage regulator ICs, two flawed ICs are allowed as shown in FIG. 1. The damaged VR components are identified by an assembly manufacturing test plan. The damaged VR components are then disabled. One method of disabling the damaged VR would be by (One time programming Nonvolatile Memory) OTP NVM programming in the VR ICs themselves. Another option is to disable the damaged VR ICs through the ENABLE pin of each VR by an on-board system controller–based manufacturing testing report. A third option is to mark the damaged components and use this marking to disable them by the on-board system level controller.

Currently, this method assumes that the order of the voltage regulator ICs does not constrain the system. It also assumes that a single VR IC yield is 0.98% and that 30 VR ICs are needed on the package to power the ASIC. In the example of two allowed flawed ICs as shown in FIG. 1, a constraint may be that the two flawed ICs cannot be adjacent in their placement or not on the same side of the ASIC, in which case the yield may drop to a value below that of the unconstrained case. An alternative implementation to increase the cumulative yield on ASICs is to combine several voltage regulator ICs into a single IC so that the total IC count is reduced and no redundancy is needed. For example, if the 30 voltage regulators ICs can be merged into two large ICs comprising 15 small ICs, it will improve the yield from 55% to 96%, assuming the assembly yield is the same for small and larger ICs, as shown in the calculation below.

Cumulative assembly yield calculation:

- 30 ICs placed. No flawed ICs allowed.
  Yield is: $0.98^{30} = 55\%$
- 31 ICs placed. One flawed IC allowed.
  Yield is: $0.98^{31} + \binom{31}{1} * 0.98^{30} * 0.02$ = 87%
- 32 ICs placed. Two flawed IC allowed (See picture below).
  Yield is $0.98^{32} + \binom{32}{1} * 0.98^{31} * 0.02 + \binom{32}{2} * 0.98^{30} * 0.02^2$= 97%

The main advantage of the method disclosed is that it trades 3% of package area and cost for more than 30% improvement in cumulative assembly yield. Another advantage is that it allows a degree of freedom in selecting the die size and power rating of the voltage regulator IC.